International Space Power System Interoperability Standards (ISPSIS)

Draft C – February 2018

REVISION AND HISTORY

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PREFACE

INTERNATIONAL SPACE POWER SYSTEM INTEROPERABILITY STANDARDS

This electrical power quality standard is to ensure commonality, reliability, interchangeability, and interoperability for electrical load applications between space power systems that will enable on-orbit or surface crew operations and joint collaborative endeavors utilizing different spacecraft systems.

Configuration control of this document is the responsibility of the International Space Station (ISS) Multilateral Coordination Board (MCB), which is comprised of the international partner members of the ISS. The National Aeronautics and Space Administration (NASA) will maintain the International Space Power System Interoperability Standards under Human Exploration and Operations Mission Directorate (HEOMD). Any revisions to this document will be approved by the ISS MCB.

INTERNATIONAL SPACE POWER SYSTEM INTEROPERABILITY STANDARDS

CONCURRENCE

FEBRUARY 2018

Associate Administrator Human Exploration and Operations NASA	Date
Executive Director, Human Space Programs State Space Corporation “Roscosmos”	Date
Director of Human Spaceflight and Operations European Space Agency	Date
Director General, Space Exploration Canadian Space Agency	Date
Executive Director Japan Aerospace Exploration Agency	Date

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1.0 INTRODUCTION

This International Space Power System Interoperability Standards is the result of a collaboration by the International Space Station (ISS) membership to establish, interoperable interfaces, terminology, techniques, and environments to facilitate collaborative endeavors of space exploration in cis-Lunar and deep space environments.

Standards that are established and internationally recognized have been selected where possible to enable commercial solutions and a variety of providers. Increasing commonality while decreasing unique configurations has the potential to reduce the traditional barriers in space exploration: overall mass and volume required to execute a mission. Standardizing interfaces reduces the scope of the development effort and allows more focus on performance instead of form and fit.

The information within this document represents a set of parameters enveloping a broad range of conditions, which if accommodated in the system architecture support greater efficiencies, promote cost savings, and increase the probability of mission success. These standards are not intended to specify system details needed for implementation nor do they dictate design features behind the interface, specific requirements will be defined in unique documents.

1.1 PURPOSE AND SCOPE

The purpose of this 120-Volt class electrical power standard is to define a bus voltage power quality, and grounding approach to ensure commonality, reliability, interchangeability, and interoperability for load applications between space application power systems such as orbital habitats, crewed or non-crewed space vehicles, ascent/descent vehicles, and surface systems. Commonality in basic equipment (lights, fans, and computers) reduces the need for unique spares that reduces the overall spare mass allocation and required stowage volume. This has a tangible impact on module size and the ultimate mass of the launch vehicle payload. A higher voltage standard provides an additional architecture level efficiency due to the mass savings it provides with the reduced conductor size required to transfer the same amount of power relative to a lower voltage system.

This standard defines the requirements and characteristics of electrical power for spacecraft. This standard also defines analysis, verification, and testing methodologies to be used to ensure that the loads operate when connected to the specified power quality and performance as defined by this standard. Utilizing this power standard, a power quality specification can then be developed that includes the detailed design performance of both the EPS and the EPCE.

The convention used in this document which indicates requirements, goals, and statements of facts is as follows: "Shall" -- Used to indicate a requirement which must be implemented and its implementation verified; "Should" -- Used to indicate a goal which must be addressed by the design but is not formally verified; "Will" -- Used to indicate a statement of fact and is not verified.

1.2 RESPONSIBILITY AND CHANGE AUTHORITY

Any proposed changes to this standard by the participating partners of this agreement shall be brought forward to the Power committee for review.

Configuration control of this document is the responsibility of the International Space Station (ISS) Multilateral Coordination Board (MCB), which is comprised of the international partner members of the ISS. The National Aeronautics and Space Administration (NASA) will maintain the Power Standards under Human Exploration and Operations Mission Directorate (HEOMD). Any revisions to this document will be approved by the ISS MCB.

1.3 PRECEDENCE

This paragraph describes the hierarchy of document authority and identifies the document(s) that take precedence in the event of a conflict between content. Applicable documents include requirements that must be met. If a value in an applicable document conflicts with a value here, then the MCB will need to resolve the issue.

Reference documents are either published research representing a specific point in time, or a document meant to guide work that does not have the full authority of an Applicable document. If a value in this document conflicts with a value in a referenced document, then it should be assumed that the value here was deliberately changed based on new data or a special constraint for the missions discussed.

2.0 DOCUMENTS

2.1 APPLICABLE DOCUMENTS

The following documents include specifications, models, standards, guidelines, handbooks, and other special publications. Applicable documents are levied by programs with authority to control system design or operations. The documents listed in this paragraph are applicable to the extent specified herein. Inclusion of applicable documents herein does not in any way supersede the order of precedence identified in Section 1.3 of this document.

None

2.2 REFERENCE DOCUMENTS

The following documents contain supplemental information to guide the user in the application of this document. These reference documents may or may not be specifically cited within the text of this document.

MIL-STD-461 G	Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment
SAE AS5698	Space Power Standard

3.0 POWER QUALITY STANDARD FOR 120VDC

3.1 GENERAL

The requirements and verifications are defined for a 120Vdc class power. The general intent is to maximize the compatibility of the EPCE across differing interfaces by broadening selected EPCE operating requirements. This standard is generic and while it can ensure compatibility on most parameters, it is limited in areas such as defining specific design impedance requirements that are needed to complete a specific design.

3.1.1 DESCRIPTION

The electrical requirements are grouped into two categories:

- Electrical Power System, Source Power Interface (section 3.3.1)
- Electric Power Consuming Equipment Interface (section 3.3.2)

Matching verifications for each of the above requirements are defined in section 3.4.

3.1.2 ENGINEERING UNITS OF MEASURE

N/A

3.2 INTERFACES

This standard is design neutral and only defines the ‘generic’ interface of the power source and of the electric power consuming equipment, and assumes it to be the same interface (see Generic Power Interface for Source/EPCE figure). An actual specific design may incorporate multiple interfaces both within the EPS or EPCE with tiered requirements that include performance margins above the next lower tier. The tiered interfaces with performance margins are defined within other documentation, such as the power quality specifications and the interface requirements documents. One of the primary goals of this standard is to maximize the use of the EPCE at all defined EPCE interfaces.

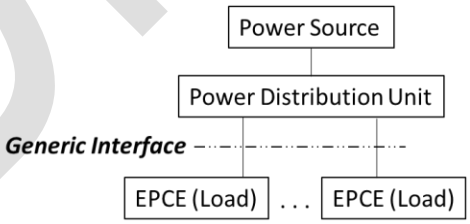


FIGURE 1 GENERIC POWER INTERFACE FOR SOURCE/EPCE

3.3 PERFORMANCE

3.3.1 ELECTRICAL POWER SYSTEM, SOURCE POWER INTERFACE

The following sections specify the characteristics for electric power supplied to electrical loads.

The EPS consists of the electric power-generating source (e.g., generators, batteries, fuel cells, solar arrays, and distribution subsystems) including the associated cables, switches, protective devices, converters, and regulators.

Power quality is directly related to the effects produced by power generation, power conditioning, system impedance, and the interactions within the distribution system which includes loads. Interactions include electromagnetic interference (EMI), regenerative energy, and system transients resulting in power surges and spikes.

3.3.1.1 EPS SYSTEM CHARACTERISTICS

3.3.1.1.1 SINGLE-POINT GROUND

[PQSV1001] A single-point ground shall be established for each EPS system.

Rationale: Establish a consistent internal grounding philosophy. This is a proven practice and consistent with heritage designs. The single-point grounding should be employed with the return lines grounded to the vehicle structure at a single point. The main characteristics of this concept are:

- The spacecraft structure is used as a low-impedance equipotential ground plane.
- No current intentionally flows through the spacecraft structure.
- All primary power sources are referenced to a single point on the spacecraft structure.
- Primary power sources are galvanically isolated from secondary power supplies.
- Secondary power supply outputs are referenced to the housing of the unit that they supply.
- The housing of each unit is referenced to the spacecraft structure at a single point.

3.3.1.1.2 DISTRIBUTION WIRING

[PQSV1002] The EPS shall provide a two-wire power distribution system in which one wire serves as a return path for load currents.

Rationale: The wiring system is required to maintain the distributed single-point ground per requirement. The two-wire distribution system does not preclude using parallel wiring for current sharing. It is recommended to minimize spacing between power and return conductors to reduce wiring inductance. No current should intentionally flow through the spacecraft structure.

3.3.1.1.3 ISOLATION

[PQSV1003] The EPS feeders and returns from multiple internal sources shall be isolated.

Rationale: Isolation of power sources will be implemented such that a fault in one source will leave the other source operational. The isolation requirement is based on the distributed single-point ground and 1 MΩ hardware configuration end item (box level) isolation requirements. No single failure within the EPS or EPCE will cause the independent power buses to lose electrical isolation. Isolation also prevents circulating AC or DC current in the EPS and/or spacecraft structure.

3.3.1.1.4 REVERSE CURRENT

[PQSV1004] The EPS shall not be required to accept EPCE (Load) reverse current flow under normal operation for a fixed interface voltage.

Rationale: Loads will be designed to prevent current to out-flow into the power system under normal load operation, on/off where the EPS voltage remains constant. Loads, mainly motors and other inertial loads need to be designed as to not normally supply reverse currents (re-gen) into the distribution system and potentially raise the bus voltage to unacceptable levels causing the unintended tripping from other devices within the system. Ripple current is controlled by the EMI control plan.

3.3.1.1.5 STABILITY

Power system stability is the ability of an electric power system to return to a state of operating equilibrium within a specified time after being subjected to a physical disturbance. The EPS will remain stable over the entire range of power generation, energy storage, and load conditions in all operating modes, temperatures, and orbital phases or conditions over the power system's design life to maintain power quality. The following section addresses the requirements to assure the bus interface stability.

3.3.1.1.5.1 SOURCE IMPEDANCE

[PQSV1005] The EPS source impedance at the EPCE interface terminals shall be established for the power system.

Rationale: The source impedance value is required to calculate the stability margin of the source/load combination at the user input terminals. This document addresses a generic interface where the EPS and the EPCE have one common interface. Specific designs most likely will have multiple tiered interfaces between the EPS and the EPCE as discussed in paragraph 3.2 and the EPS impedance will be determined at each defined interface.

3.3.1.1.5.2 SMALL SIGNAL STABILITY – SYSTEM STABILITY

[PQSV1006] A complex impedance margin shall be maintained for the source impedance divided by the load impedance ratio that remains outside the hatched area (Forbidden Zone) shown in the EPS Nyquist Stability Criteria figure.

Rationale: This Nyquist Criteria was adopted as a system level stability check. In general, this standard has been assembled with supply side and load side requirements so that the EPS and loads can be developed separately. This criterion uses design data from both the supply and load as the ultimate overall stability check. The approach is based on the significant relationship between source and load impedance and the effect of this relationship on system stability. The stability criteria establish that maintaining a 3 dB (0.707) impedance margin between unity gain and the ratio of source and load impedance provides system stability. When the margin for impedance magnitude is less than 3 dB, then the phase margin cannot enter the Forbidden Zone shown in the Nyquist Stability Plot of |ZS divided by ZL| figure over the span of frequencies from 30 Hz to 100 kHz. The application of the stability criteria should consider all possible source and loads combinations that may occur, including the failure of any equipment connected to the bus. On the Nyquist plot, the phase margin is specified only at the cross-over points where ZS divided by ZL intersects the unit circle. The stability criteria are discussed further in the General Discussion appendix of this document. Maintaining stability is especially important to maintaining power quality in a multiple load and multiple channel system because instability in any part of the system will cause degradation, if not a total loss, to the power quality delivered to any other part of the system.

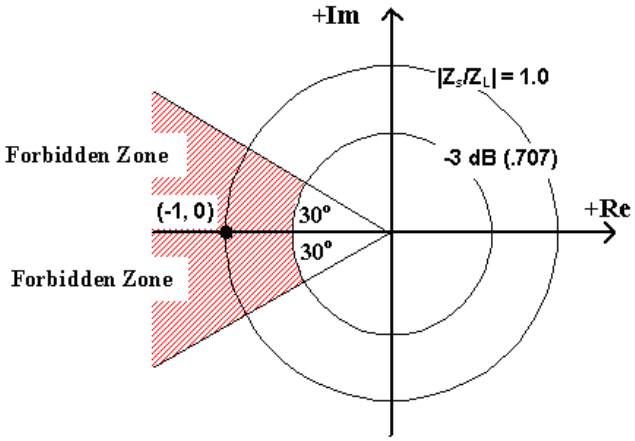


FIGURE 2 EPS NYQUIST STABILITY CRITERIA

NOTE:

1. Z_S is the output impedance of the source subsystem.
2. Z_L is the input impedance of the load subsystem.

3.3.1.1.6 ELECTROMAGNETIC COMPATIBILITY

[PQSV1007] An EPS EMI control plan shall be established in accordance with the vehicle mission requirements.

Rationale: Adopt a common Electromagnetic Interference (EMI) requirement for the power system.

3.3.1.2 NORMAL OPERATION REQUIREMENTS

The electrical power system provides the following system power quality in the absence of failures or fault conditions.

3.3.1.2.1 STEADY STATE VOLTAGE

[PQSV1008] The EPS shall supply the steady-state voltage at the EPS/EPCE interface within the range of 98 to 136 Vdc for load conditions from no load to rated capacity of the system.

Rationale: Establish a system voltage range for the EPS at the input terminals of a load to account for the voltage drops throughout the EPS and stay within the prescribed nominal steady-state voltage. The voltage ranges include the expected voltage swing for a power system that is comprised of batteries and either solar arrays or fuel cell power generation with nominal voltage losses due to the EPS distribution system. It is important to note that this defines the generic EPS/EPCE load interface voltage. Other upper tier EPS system interface voltages may be defined at other areas within the overall EPS system and require voltage performance margins to be added.

3.3.1.2.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

[PQSV1009] The electric power shall remain within the magnitude and duration limits for voltage transients shown in the 120V EPS Normal Transient Response figure.

Rationale: This requirement establishes a normal operating magnitude limit for voltage transients for an EPCE interface due to normal switching of loads that will provide sufficient operational voltage margin for the downstream EPCE. This power envelope may differ from the main power bus transient. Extreme high and low bus voltages are assumed contingency cases, and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. It is important to note that this defines the generic EPS/EPCE load interface performance. Other upper tier EPS system interfaces may be defined at other areas within the overall EPS system and require performance margins to be added.

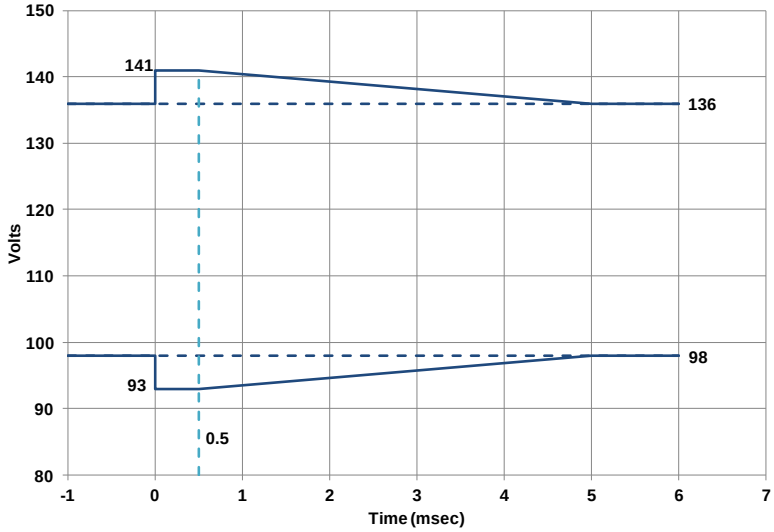


FIGURE 3 120V EPS NORMAL TRANSIENT RESPONSE

NOTE: The envelope shown applies to the transient responses exclusive of any periodic noise components that may be present.

3.3.1.2.3 RIPPLE VOLTAGE

Ripple voltages are superimposed on the power system and can dramatically affect instrumentation and other sensitive loads. The ripple voltage is a primary power quality parameter. The total system ripple voltage is comprised of the collective contributions from sources and loads. Design specific power specifications may allocate the ripple for the EPS itself at specified upper tier EPS interfaces, including the generic EPS/EPCE interface. Ripple is defined by three requirements, peak voltage, ripple voltage amplitude, and ripple voltage spectrum.

3.3.1.2.3.1 PEAK RIPPLE VOLTAGE

[PQSV1010] The peak ripple voltage shall be less than 10.0 Vp-p (peak-to-peak) in a bandwidth of 30Hz to 1 Mhz.

Rationale: Establish a worst-case peak system ripple voltage with the collective contributions from sources and loads. The requirement particularly targets ripple voltage contributions generated by pulses, doublet pulses and spike waveforms.

3.3.1.2.3.2 RIPPLE VOLTAGE AMPLITUDE

[PQSV1011] The ripple voltage amplitude shall be less than 3.0 Vrms in a bandwidth of 30 Hz to 1 MHz.

Rationale: Establish a worst-case maximum system ripple voltage as a primary power quality parameter. This requirement limits the total rms voltage composite of all ripple harmonics. The requirement particularly targets ripple voltage contributions generated by low frequency, non-harmonic, and pulsed loads.

3.3.1.2.3.3 RIPPLE VOLTAGE SPECTRUM

[PQSV1012] The frequency distribution of the ripple voltage shall remain within the limits shown in 120V Ripple Voltage Spectral Components figure.

Rationale: Establish a worst-case system ripple voltage characterized against a frequency range with collective contributions from sources and loads. This system ripple spectrum defines power quality for the electromagnetic emissions and susceptibility requirements. This spectrum requirement limits ripple voltage contribution generated by periodic waveforms such as sine, square and triangle waves.

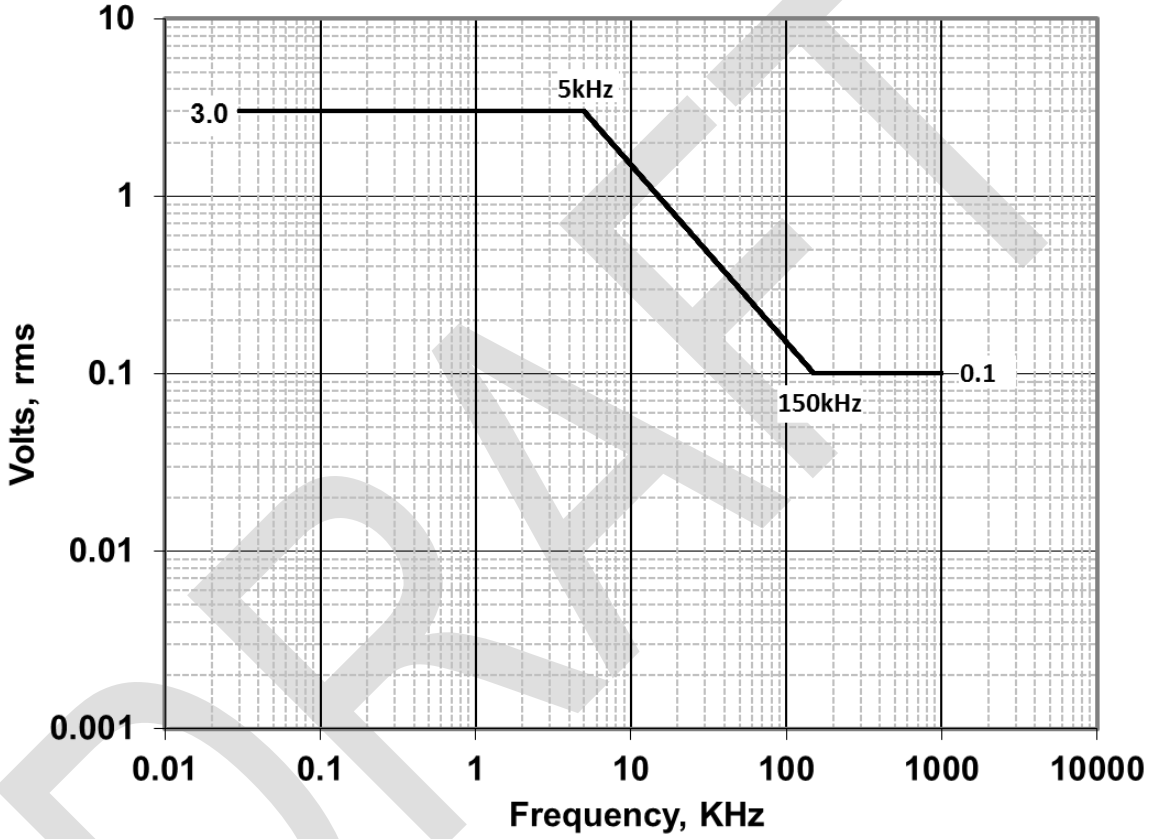


FIGURE 4 120V RIPPLE VOLTAGE SPECTRAL COMPONENTS

3.3.1.2.4 EXTERNAL POWER SOURCE

[PQSV1013] External electric power sources shall supply power having the characteristics as specified within this standard.

Rationale: External power (any auxiliary or emergency power) must maintain the same ripple, transient, stability, isolation and fault coordination characteristics that the EPS maintains regardless of whether the external power is operating stand-alone or integrated with the power system.

3.3.1.2.5 INRUSH/SURGE CURRENT TRANSIENTS

[PQSV1014] The EPS shall support load inrush/surge currents of:

- 0.012 ampere-seconds / ampere for loads with currents 0A < i < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < i < 200A

*Rationale: Establish inrush/surge capability for the power source. EPS designers must allow for inrush/surge conditions while maintaining nominal system voltage. While this inrush/surge requirement does not take into account source / load margin, the EPS designers need to determine sufficient margins to avoid nuisance tripping of source switchgear from protection circuits. Designers should consider minimum values of margin of 120% of rated output when connecting loads that are not predetermined. The ampere-seconds/ampere are normalized inrush ampere-second current divided by the source current rating of the source. The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000uF for a 10 Amp source at 120V as determined by the equation C = Q/V: C = 0.012sec*10A/120V = 1000μF or since the 10A source is also valid for the second equation: ((0.00253sec*10A) + 0.0947) / 120V = 1000 μF.*

EPS designs may require additional power conditioning for a large inrush condition to limit the bus voltage drop.

3.3.1.3 ABNORMAL OPERATION

The electrical power system provides the following system power quality in the presence of failures or fault conditions.

3.3.1.3.1 ABNORMAL REVERSE CURRENT

[PQSV1015] The EPS shall accept reverse currents under abnormal conditions without damage.

- 0.012 ampere-seconds / ampere for loads with currents 0A < i < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < i < 200A

*Rationale: Establish a minimum reverse current capability for switchgear servicing loads during voltage droop due to EPS transients or a system fault condition to avoid damaging the switchgear. The reverse current source is the discharge of load input filter capacitors into the faulted EPS. The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000uF for a 10 Amp source at 120V as determined by the equation C = Q/V: C = 0.012sec*10A/120V = 1000μF or since the 10A source is also valid for the second equation: ((0.00253sec*10A) + 0.0947) / 120V = 1000 μF.*

3.3.1.3.2 EPS FAULT PROTECTION

[PQSV1016] The EPS power distribution system shall provide overcurrent protection to branch circuits to limit fault currents and isolate faults.

Rationale: The requirement establishes a consistent fault mitigation method for the EPS interface to the EPCE. Faults in any load branch must be cleared and not cause any other load to become disabled. The protection should limit/clear the overcurrent condition to maintain the EPS power quality.

3.3.1.3.3 OVERVOLTAGE SURGE

[PQSV1017] The EPS source at the EPCE interface shall recover from an overvoltage surge due to an EPS fault condition to within power quality as shown in the EPS Abnormal Limits for Overvoltage and Undervoltage figure.

Rationale: Establish a worst-case overvoltage condition at the EPCE interface during fault clearing from EPS failures. This condition is produced from stored energy within the power distribution system and loads. Power system designers need to select hardware to withstand anticipated worst-case overvoltage without damaging parts of the power system. It must be noted that this event is defined at the EPCE interface.

This condition is produced from stored energy within the power distribution system and loads. Power system designers need to select hardware to withstand anticipated worst-case overvoltage without damaging parts of the power system.

3.3.1.3.4 UNDERVOLTAGE SURGE

[PQSV1018] The EPS source shall recover from an undervoltage surge due to an EPS fault condition to within power quality as shown in EPS Abnormal Limits for Overvoltage and Undervoltage figure.

Rationale: Establish a worst-case undervoltage condition for the EPS at the EPCE interface, experienced from fault clearing. This condition depends on the location of the fault in the load distribution power system and where it is observed. Clearing of load faults generally will not induce conditions as severe and distribution switchgear that limits fault currents closer to the EPCE minimizes the effects of system faults. The undervoltage condition will fall outside the normal operating voltage, (as low as zero volts), clear the condition, reconfigure, and return to within power quality. Power quality will be re-established for users outside of the faulted area. Power system designers need to select hardware to withstand anticipated worst-case undervoltage conditions without damaging parts of the power system. This requirement does not intend to specify that any part of the power system will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. Other considerations such as criticality or system operational modes need to be used to determine recovery state. It must be noted that this event is defined at the EPCE interface.

Consider criticality or system operational modes when determining recovery state.

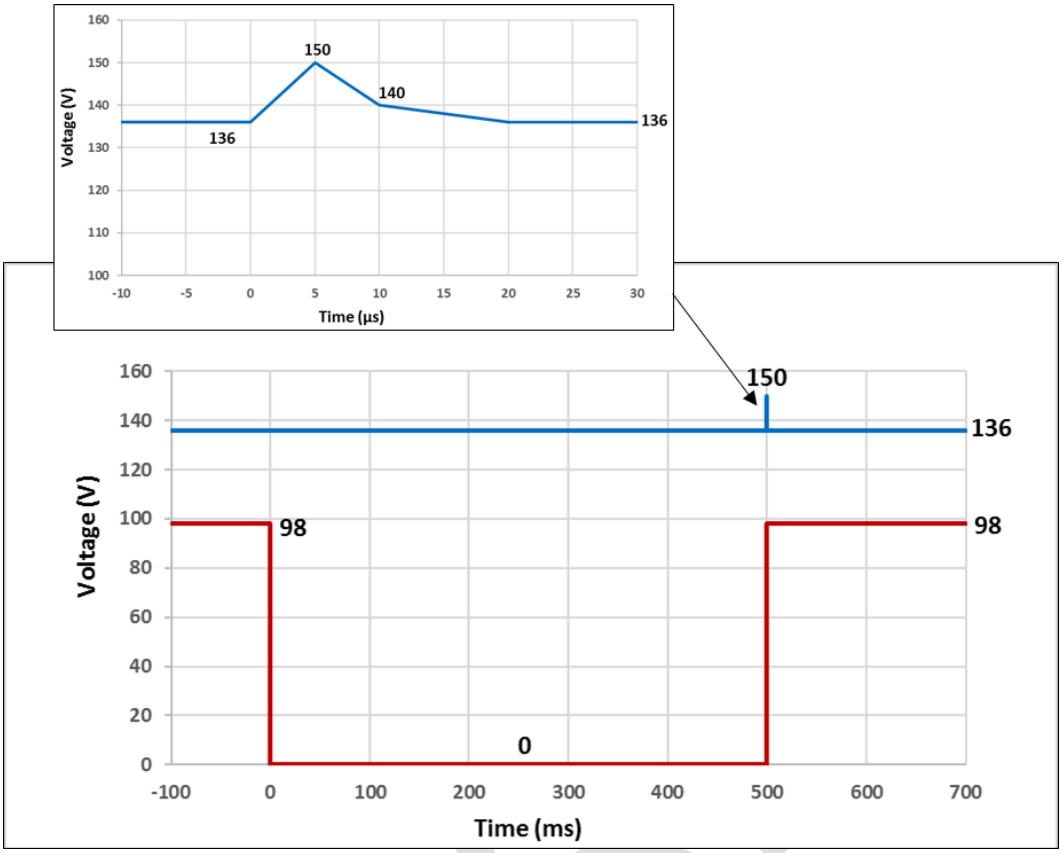


FIGURE 5 120V EPS ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.3.1.3.5 EMERGENCY OPERATION

[PQSV1019] The EPS shall be capable of supplying power until all energy sources are depleted.

Rationale: The EPS should provide for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization.

3.3.1.3.6 FAULTS

Abnormal conditions occur when a system malfunctions or a fault/failure of the EPS occurs. The protective devices of the EPS during this condition operate to isolate or remove the faulted system from the appropriate EPS interface and recover/reconfigure from the fault/failure. Under abnormal conditions, the power quality will not be maintained. Power system designs must take into account these major system fault conditions.

3.3.1.3.6.1 HIGH IMPEDANCE FAULTS

[PQSV1020] The EPS shall isolate high impedance faults (soft faults) for overcurrent conditions in excess of 150% of rated current of the upstream protective device for a maximum total clearing time less than 4 seconds (from time of detection).

Rationale: Establish a worst-case clearing time constraint for overcurrent conditions that stress the overall distribution system. The overcurrent conditions must be removed from the EPS. Clearing times for various loads will be based on mission requirements, criticality of the load, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics.

3.3.1.3.6.2 HIGH CURRENT FAULTS

[PQSV1021] The EPS shall isolate high current faults (short circuit) for overcurrent conditions in excess of 400% of the rated current of the upstream protective device with a maximum total clearing time less than or equal to 15 ms (from time of detection).

Rationale: Establish a worst-case clearing time for high current faults (short circuit or a load resistance that produces equivalent 400% load current) type conditions that stress the distribution system. Short circuit conditions have to be removed quickly from the EPS before damaging other areas of the system. Faster clearing times under these conditions will be based on mission requirements, criticality of the loads, and switchgear requirements. The intent of this requirement is to constrain fault current conditions and not directly define the switchgear characteristics.

3.3.1.3.6.3 EPS, FAULT CONTAINMENT

[PQSV1022] The EPS shall provide fault protection coordination so that the protective circuit closest to the fault will contain an electrical short circuit in the electrical distribution system.

Rationale: Establish fault coordination as fundamental in maintaining the operability of the power system while isolating failures and minimizing the impact of failures to the remaining power system at the EPS. Fault coordination across the interface is necessary to ensure that load branch faults will be cleared without affecting any other load. Coordination must take into account upstream protective equipment, stored energy causing damaging currents, and inrush currents during fault recovery. This coordination will also be implemented downstream from current limiting switchgear to isolate faults occurring in any of the power controller's output lines to contain the fault so the device closest to the fault trips first and power can continue to be provided to the remaining unfaulted outputs. Overcurrent protection should be located at the output of the distribution system. The overcurrent protection will isolate a particular branch feed from the power system. Select overcurrent devices based on the overall protection coordination.

3.3.2 ELECTRIC POWER CONSUMING EQUIPMENT INTERFACE

The following requirements are imposed on each electric power load to guarantee the required EPS power quality is maintained. The electrical power characteristics specified herein are minimum requirements for EPCE electrical loads. An EPCE constitutes every fixed or portable device that consumes electric power. The following paragraphs describe the requirements on electrical users. The performance is specified at the input terminals of individual EPCEs (electrical loads).

3.3.2.1 NORMAL OPERATION

The following requirements cover normal operations of EPCEs in the absence of failures or fault conditions.

3.3.2.1.1 STEADY STATE OPERATION

[PQSV2001] EPCE shall operate with an input voltage within the range of 98 to 136 Vdc.

Rationale: This voltage is defined at the input terminals of the EPCE. The EPCE are designed to operate within the full range of the voltage parameter to allow voltage compatibility across multiple interfaces as discussed in paragraph 3.2.

3.3.2.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

[PQSV2002] The EPCE shall operate within the EPS system voltage transient limits defined in 120V EPS Normal Transient Response figure.

Rationale: The 120V EPS Normal Transient Response figure shows the normal operating magnitude and duration limits for voltage transients at the EPCE power interface due to normal switching of loads. The transient range does not take into account any margins that system designers need to take into account in the load design. The extreme high and low bus voltages are assumed contingency cases and while experiencing these conditions it is assumed that the power system will experience small changes in load steps. This power envelop may differ from the main power bus transient. The EPCE must operate nominally anywhere within the upper and lower boundary condition.

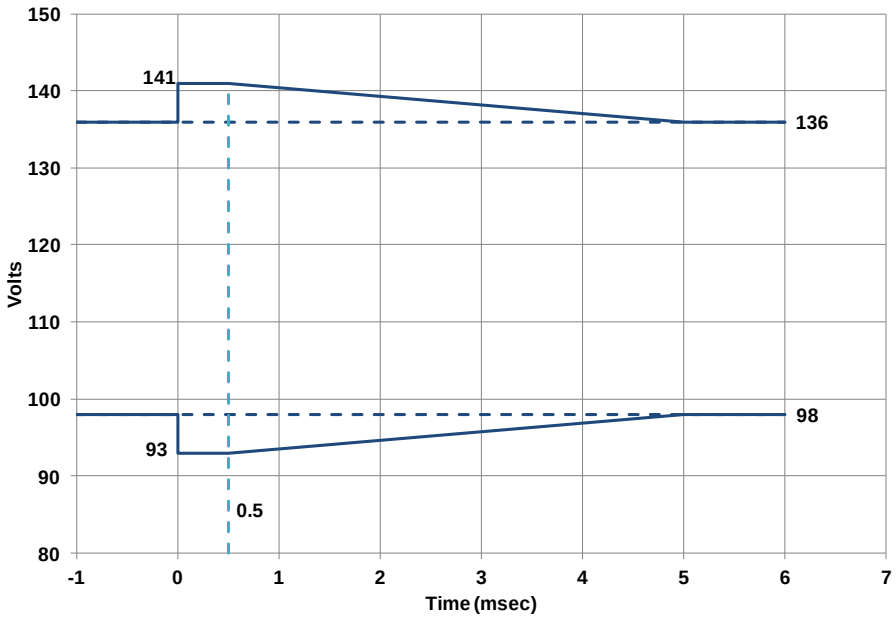


FIGURE 6 120V EPCE NORMAL TRANSIENT RESPONSE

NOTE: The envelope shown applies to the transient responses exclusive of any periodic noise components that may be present.

3.3.2.1.3 EPCE, RIPPLE CURRENT

[PQSV2003] EPCEs shall meet the emissions limits as set by the EMI control plan.

Rationale: Ripple currents and voltages are superimposed on the 120Vdc and can have dramatic effects on instrumentation and other sensitive loads. The total system ripple voltage is the collective contributions from sources and loads. EPCEs must minimize ripple contribution to the system.

3.3.2.1.3.1 EPCE, RIPPLE VOLTAGE SPECTRUM

[PQSV2004] EPCE shall operate nominally and maintain stability when subjected to the ripple spectrum as specified in the EMI control plan.

Rationale: Requirements analogous to CS101 of MIL STD 461 are defined as the worst-case system ripple voltage for EPCE power interface as a primary power quality parameter. Ripple voltage is characterized against frequency range and describes the worst-case ripple voltages with collective contributions from sources and loads. This system ripple spectrum is a basic power quality requirement and is the basis for the electromagnetic susceptibility requirements. Ripple voltages are shown as a maximum, which include the system ripple voltage and the EPCE ripple voltage introduced by a load. The system ripple voltage does not take into account any margins that system designers need to apply to the load design. This spectrum susceptibility requirement encompasses the ripple voltage contribution generated by periodic waveforms such as sine, square, and triangle waves.

3.3.2.1.4 STABILITY

3.3.2.1.4.1 LOCAL STABILITY

Local stability refers to the stability of a load with respect to a representative source (not necessarily the EPS). Meeting the requirements of the following sections assures a margin of stability for the loads. Stability is essential to maintain power quality for system loads. These requirements need to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same power domain.

3.3.2.1.4.1.1 LARGE SIGNAL STABILITY

[PQSV2005] The EPCE shall provide a transient response that is damped as shown in Large Signal Stability Transient Response figure when subjected to short-duration source-side transient voltages as defined in [PQSV2005V] (paragraph 3.4.2.1.4.1.1).

Rationale: The transient response must decay and remain below 10 percent of the maximum response amplitude within 1.0 milliseconds as illustrated in the Large Signal Stability Transient Response figure. The time to damp to 10 percent, as shown, is also referred to as settling time.

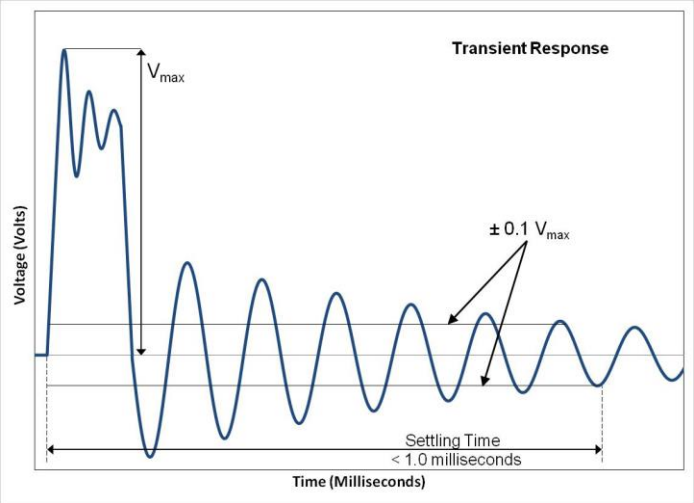


FIGURE 7 LARGE SIGNAL STABILITY

3.3.2.1.4.1.2 EPCE INPUT IMPEDANCE

[PQSV2006] The EPCE input load impedance at the EPCE interface terminals shall be established.

Rationale: The EPCE impedance value is required to calculate the stability margin of the source/load combination at the user input terminals. This document addresses a generic interface where the EPS and the EPCE have one common interface.

3.3.2.1.4.1.3 SMALL SIGNAL STABILITY

[PQSV2007] The EPCE shall maintain a complex impedance ratio of source impedance divided by load impedance (derived from [PQSV 1005] paragraph 3.3.1.1.5.1) that remains outside the hatched area (Forbidden Zone) shown in Nyquist Stability of Plot ZS divided by ZL figure, from 30 Hz to 100 kHz for all defined EPCE interfaces.

Rationale: The EPCE should meet this system level requirement for Small Signal Stability for all defined EPCE interfaces to maximize compatibility.

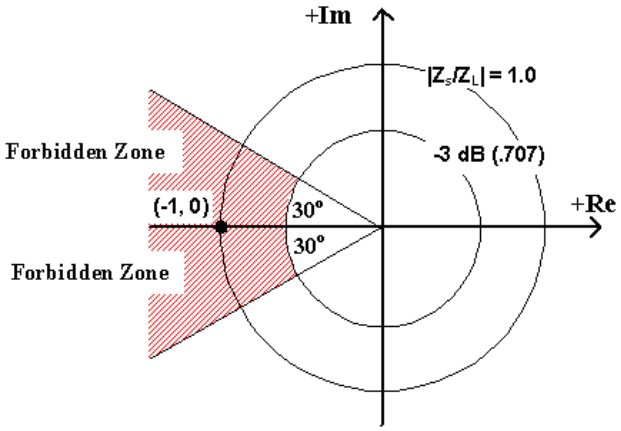


FIGURE 8 NYQUIST STABILITY OF PLOT ZS/ZL

NOTE:

1. Z_S is the output impedance of the source subsystem.
2. Z_L is the input impedance of the load subsystem.

3.3.2.1.5 STARTUP AND INRUSH

3.3.2.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

[PQSV2008] An EPCE shall be capable of operating from current limiting switchgear.

Rationale: Switchgear may limit the maximum input current to a value near the channel rating. EPCE with large values of energy storage (in capacitive filters or equivalent) will extend the rise time of the applied voltage as these filters charge. In extreme cases, the charging time may be greater than 100 msec. The EPCE must be compatible with this slow rise time.

3.3.2.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

[PQSV2009] An EPCE shall limit Inrush/Surge current to:

- 0.012 ampere-seconds / ampere for loads with currents 0A < i < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < i < 200A

*Rationale: Loads must limit current transients to within safe operating limits of the upstream switch with trip characteristics. The normalized ampere-seconds/ampere units are defined as the inrush ampere-second current divided by the rated load current. Load current transients must be coordinated with upstream switchgear. The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000uF for a 10 Amp load at 120V as determined by the equation C = Q/V: C = 0.012sec*10A/120V = 1000μF or since the 10A load is also valid for the second equation: ((0.00253sec*10A) + 0.0947) / 120V = 1000 μF.*

3.3.2.1.6 REVERSE CURRENT

[PQSV2010] The EPCE shall not produce reverse current flow back into the EPS source under normal operation for a fixed interface voltage.

Rationale: EPCEs need to be designed to prevent current to out-flow into the power system under normal load operation with the voltage remaining constant. Loads, mainly motors and other inertial loads need to be designed as to not normally supply reverse currents (re-gen) into the distribution system and potentially raise the bus voltage to unacceptable levels causing the unintended tripping from other devices within the system. This requirement assumes a fixed steady state EPS bus voltage without any EPS droop in voltage therefore it is assumed that energy storage devices such as capacitors will not be affected by this requirement.

3.3.2.1.7 EPCE INPUT ISOLATION

[PQSV2011] The EPCE shall provide a minimum of 1 MΩ DC-resistive input isolation and also maintain isolation between each independent source input and between each source and chassis.

Rationale: Maintain a consistent level of input isolation for EPCE and maintain isolation between power inputs such that no single failure within the EPCE will cause loss of electrical isolation between independent power buses or to chassis ground. These requirements apply to both supply and return circuits. Return isolation needs to be maintained when there are multiple circuits so as to not create a loop path (antenna), multiple return path (currents flowing through the single-point ground), or common mode currents. Isolation from chassis must be maintained to prevent currents through vehicle structure. Each EPCE must meet the failure requirements of the vehicle and should not cause loss of isolation between independent power busses.

3.3.2.2 ABNORMAL OPERATION

The EPCE is to return to normal operations after experiencing abnormal transients due to fault clearing identified in the following paragraphs. Abnormal transients occur when a malfunction or fault/failure is present in the system. The protective devices of the EPS, during this condition, operate to isolate or remove the fault from the appropriate EPS interface and recover from the fault/failure.

3.3.2.2.1 ABNORMAL REVERSE CURRENTS

[PQSV2012] The EPCE shall limit reverse currents under abnormal conditions to:

- 0.012 ampere-seconds / ampere for loads with currents 0A < i < 10A
- 0.00253 A*Sec / A + 0.0947 for loads with currents 10A < i < 200A

Rationale: Determine safe levels of reverse current that an EPCE can provide during an EPS voltage droop or fault condition to ensure that the currents do not raise the bus voltage to unacceptable levels and potentially damage the distribution system switchgear. The ampere-seconds/ampere units are defined as the reverse current ampere-second current divided by the rated load current. EPS switchgear and

*protection is limited in the amount of reverse current that can be supplied by the loads. The value of 0.012 ampere-seconds/ampere is equivalent to a capacitance of 1000uF for a 10 Amp load at 120V as determined by the equation C = Q/V: C = 0.012sec*10A/120V = 1000µF or since the 10A load is also valid for the second equation: ((0.00253sec*10A) + 0.0947) / 120V = 1000 µF.*

3.3.2.2.2 OVERVOLTAGE SURGE

[PQSV2013] The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing an overvoltage due to an EPS fault as shown in EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage figure.

Rationale: This defines a worst-case overvoltage condition during fault clearing for major EPS faults. The user should not expect power quality during a fault condition. EPCE designers must take into account these conditions in the design of loads. EPCE designers need to select hardware to withstand anticipated worst-case overvoltage without permanently damaging system loads. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart.

3.3.2.2.3 UNDERVOLTAGE SURGE

[PQSV2014] The EPCE shall meet the operational performance requirements as defined by the EPCE controlling documents after experiencing undervoltage due to an EPS fault as shown in EPCE Abnormal Voltage Limits for Overvoltage and Undervoltage figure.

Rationale: This event is defined at the EPCE interface. The user should not expect power quality during an EPS fault condition. The worst-case undervoltage condition will be outside of power quality while the system detects the fault, clears the condition, and re-establishes power to within power quality. Power quality will be re-established for users outside of the faulted area. EPCE controlling documents define how the equipment will operate nominally through the transient or recover to a safe state either automatically or by manual restart. The intent of this requirement is that loads should not be damaged or cause an unsafe condition as a result of undervoltage events. This requirement does not intend to stipulate whether any given load will be required to operate through the transient event or should configure to operate immediately following the event. The intent is to establish that the source may be removed such that all of the downstream EPCE may cease operating and will not be damaged. The EPCE input filter is not required to act as an uninterruptable power supply and any critical EPCE should have redundancy or multiple independent source inputs. Other considerations such as load criticality or system operational mode need to be used to determine recovery state. The EPCE can experience abnormal voltage droop and voltage overshoot greater than specified by the EPS, Normal Load Step Transient Voltage [PQSV1009] *paragraph 3.3.1.2.2 while sharing an EPS source interface feeder with other loads. The magnitude of the abnormal voltage will be dependent on the loads applied and being applied / removed. Determination of the effects from the switching*

disturbances will be identified by the specific hardware controlling documents. It must be noted that this event is defined at the EPCE interface.

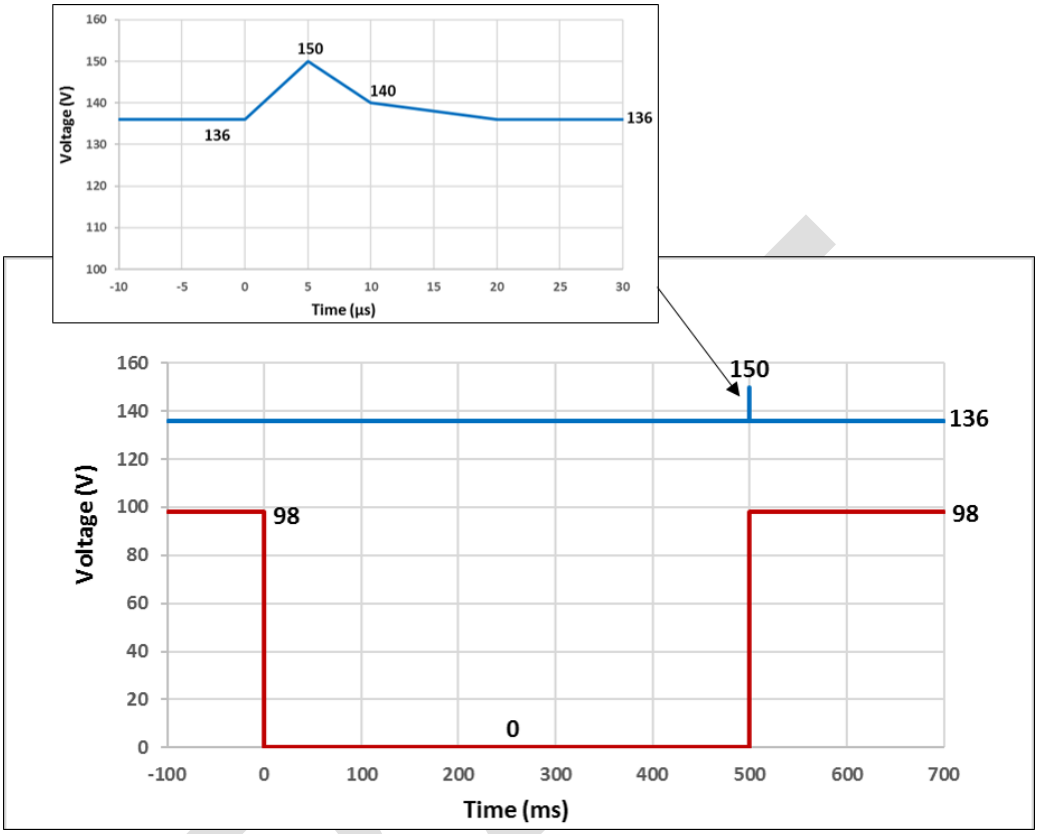


FIGURE 9 120V EPCE ABNORMAL VOLTAGE LIMITS FOR OVERVOLTAGE AND UNDERVOLTAGE

3.3.2.2.4 EMERGENCY OPERATION

[PQSV2015] EPCE deemed essential (contingency operations) shall continue to operate without loss of performance down to the reduced Emergency Voltage Limit of 95V.

Rationale: Establish an emergency operation system voltage range. The voltage allows for contingency cases where the primary power generation source is disabled or unavailable to allow for 100% power system utilization. This requirement typically applies to unregulated sources (i.e., battery) where there are a few specified EPCE that are required to continue to operate below normal minimum voltages for contingency operations. Operations below this contingency voltage is usually not practical due to the source no longer able to supply the required current for the EPCE to operate.

3.4 VERIFICATION AND TESTING

An important part of achieving reliability of the EPS is through verification performed at the appropriate level of assembly. This section is intended to identify critical electrical characteristics that need to be verified. This section provides the complete set of verification requirements necessary to ensure compliance with the interface and design requirements contained in the General Power Quality Requirements section.

The verification process and requirement closure is performed to ensure that the product complies with the requirement as specified and as determined by the verification requirement. Section 3.4 contains a verification requirement for each requirement in Section 3.3.

The intent is to establish verification of spacecraft power sources (EPS) with clean, resistive loads, and to establish verification for spacecraft loads (EPCE) with clean, battery-like sources.

A - Analysis is a method of verification utilizing techniques and tools such as computer and hardware simulations, analog modeling, similarity assessments, and validation of records to confirm that design requirements to be verified have been satisfied. Analysis is the evaluation of the results of multiple tests and analyses at a lower level as it would apply to a higher level of assembly. When analysis is selected as the verification method, the chosen analytical methodology will be supported by appropriate rationale and be detailed in the applicable documents.

D - Demonstration is a qualitative exhibition of functional performance (i.e., serviceability, accessibility, transportability, and human engineering features) usually accomplished with no or minimal instrumentation.

I - Inspection is a method of verification of physical characteristics that determines compliance of the item with requirements without the use of special laboratory equipment, procedures, test support items, or services. Inspection uses standard methods such as visuals, gauges, etc. to verify compliance with requirements. Hardware may be inspected for the following:

- Construction
- Workmanship
- Physical condition
- Specification and/or drawing compliance

Inspection may be used to confirm that engineering drawings call out proper design and construction features (e.g., materials and processes). Inspection includes Review of Design (ROD). This is typically a review of the as-built drawings to confirm that a design feature has been incorporated into the design.

T - Test is a method of verification wherein requirements are verified by measurement during or after the controlled application of functional and environmental stimuli. These measurements may require the use of laboratory equipment, recorded data, procedures, test support items, or services. For all verification, qualification, and acceptance test activities, pass or fail test criteria or acceptance tolerance bands (based upon design and performance requirements) shall be specified prior to conducting the test. This will ensure that the actual performance of tested equipment or systems meets or exceeds specifications.

3.4.1 ELECTRICAL POWER SYSTEM, SOURCE POWER INTERFACE

3.4.1.1 EPS SYSTEM CHARACTERISTICS

3.4.1.1.1 SINGLE-POINT GROUND

[PQSV1001V] Verification of single point ground shall be performed by inspection. An inspection of all production electrical wiring drawings shall be performed to verify that the power distribution system maintains a single point ground.

3.4.1.1.2 DISTRIBUTION WIRING

[PQSV1002V] Verification of two-wire distribution shall be performed by inspection. An inspection of all production electrical wiring drawings shall be performed to verify that the power distribution system maintains a two-wire system. The verification shall be considered successful when the inspection shows that the EPS utilizes a two-wire system as specified in the requirement [PQSV1001].

3.4.1.1.3 ISOLATION

[PQSV1003V] Verification of Power Bus Isolation between two or more independent EPS Power Buses shall be performed by inspection. A review of production drawings and hardware configuration end item input isolation data shall be performed to verify that the supply line of each channel and return line (excluding single-point ground connection points) of each channel are not connected together. The verification shall be considered successful when the inspection shows that the isolation between supply lines of each channel and return lines (excluding single-point ground connection points) of each channel are isolated as specified.

3.4.1.1.4 REVERSE CURRENT

NVR

Rationale: No EPS verification required under normal operations since there is no EPCE reverse current allowed. However, under abnormal operations the EPS will need to meet the EPCE abnormal reverse current as defined under requirement [PQSV1015]*.*

3.4.1.1.5 STABILITY

3.4.1.1.5.1 SOURCE IMPEDANCE

[PQSV1005V] The EPS source impedance shall be determined by test and analysis. See Appendix E.3.

3.4.1.1.5.2 SMALL SIGNAL STABILITY – SYSTEM STABILITY

[PQSV1006V] Verification of small signal stability shall be performed by analysis and test of source and load impedances. An analysis shall be performed based on the Nyquist criteria shown in requirement [PQSV1006].

3.4.1.1.6 ELECTROMAGNETIC COMPATIBILITY

[PQSV1007V] Verification shall be performed by completing the analyses and tests per EMI Control Plan in accordance with the vehicle mission requirements.

Rationale: Adopt a common Electromagnetic Interference (EMI) requirement for the power system.

3.4.1.2 NORMAL OPERATION REQUIREMENTS

3.4.1.2.1 STEADY-STATE VOLTAGE

[PQSV1008V] Verification of compatibility with the steady-state voltage range shall be performed by test.

The steady-state voltage shall be measured under a no load open circuit condition and when subjected to a resistive load at 100% of rated capacity. The verification shall be considered successful when the test shows that the EPS provided steady-state voltage is within the range specified in requirement [PQSV1008] for the EPCE power interface.

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PQSV1008] for the downstream EPCE power interface.

Rationale: Minimum load condition is the initial powered up state of the system.

3.4.1.2.2 NORMAL LOAD STEP TRANSIENT VOLTAGE

[PQSV1009V] Verification of compatibility with the normal load step transient shall be performed by test.

A test shall be performed to verify that the voltage remains within the magnitude and duration limits specified in the requirements when subjected to a 50% (±5%) representative load change including application and removal of the load with a nominal initial voltage within the range specified. The representative load shall be 50% (±5%) of the rated output power. The test shall be performed in two parts. The first part shall consist of the application and removal of the load with the EPS operating at 10% (±5%) of nominal operating mode power capacity. The second part shall consist of the application and removal of the load with the power system operating at 45% (±5%) of nominal operating mode power capacity. The verification shall be considered successful when the tests show that the voltage remains within the range specified in requirement [PQSV1009].

Any EPS power interface defined upstream of the EPCE power interface shall also include the necessary voltage drop margins to maintain the range specified in requirement [PQSV1009] for the downstream EPCE power interface.

Rationale: This normal load step test should be conducted under nominal system operating conditions and should not be considered a turn-on or turn-off transient test. The test conditions are at the loads interface.

3.4.1.2.3 RIPPLE VOLTAGE

3.4.1.2.3.1 PEAK RIPPLE VOLTAGE

[PQSV1010V] Verification of the peak ripple voltage shall be performed by test. A test shall be performed to verify that the maximum peak ripple voltage is less than limits specified in the requirements when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the maximum peak ripple voltage is less than 10.0 Vp-p (peak-to-peak) in a bandwidth of 30Hz to 1 Mhz.

Rationale: Maximum peak ripple voltage is useful as a primary power quality parameter so components can be properly sized to withstand peak voltages within the system. Loads that are to be connected to the power system are considered representative loads. This requirement is intended to be verified under lab conditions using a representative interface source and load. Design specific power specifications may allocate the ripple for the EPS itself at specified upper tier EPS interfaces, including the generic EPS/EPCE interface.

3.4.1.2.3.2 RIPPLE VOLTAGE AMPLITUDE

[PQSV1011V] Verification of the ripple voltage amplitude shall be performed by test. A test shall be performed to verify that the maximum rms ripple voltage is less than limits specified in the requirements when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the maximum ripple voltage is less than 3.0 Vrms in a bandwidth of 30 Hz to 1 MHz. This measurement shall be made using a true rms voltmeter with a bandwidth of at least 1 MHz.

Rationale: Maximum rms ripple voltage is useful as a primary power quality parameter to determine how much "ac noise" is present in the dc system. Loads that are to be connected to the power system are considered representative loads. Ripple voltage includes the collective contributions from sources and loads at EPS Interface as a primary power quality parameter. Design specific power specifications may allocate the ripple for the EPS itself at specified upper tier EPS interfaces, including the generic EPS/EPCE interface.

3.4.1.2.3.3 RIPPLE VOLTAGE SPECTRUM

[PQSV1012V] Verification of the ripple voltage spectrum shall be performed by test. A test shall be performed to verify that the ripple voltage remains within the magnitude and frequency limits specified in the requirements when subjected to resistive loads that draw 20% (±5%) and 100% (+0/-5%) of the rated power. The verification shall be considered successful when the test shows that the ripple voltage is within the range specified in requirement [PQSV1012].

Rationale: Ripple voltage is useful as a primary power quality parameter to determine how much "ac noise" is present in the dc system over a defined frequency spectrum. Ripple voltage includes the collective contributions from sources and loads at the EPS Source interface as a primary power quality parameter. The frequency domain limit of

the cumulative noise is maintained at least 6dB below the EMC conducted susceptibility requirements of MIL-STD-461. Design specific power specifications may allocate the ripple for the EPS itself at specific defined interfaces, not just at the generic EPS/EPCE interface.

3.4.1.2.4 EXTERNAL POWER SOURCE

[PQSV1013V] External power sources shall be tested to verify compliance with this standard.

3.4.1.2.5 INRUSH/SURGE CURRENT TRANSIENTS

[PQSV1014V] Verification of EPS inrush capability shall be performed by test. The test shall be performed by charging the specified equivalent capacitance without causing a trip of the controlling switchgear.

3.4.1.3 ABNORMAL OPERATION

3.4.1.3.1 ABNORMAL REVERSE CURRENT

[PQSV1015V] Verification that the EPS can accept the abnormal EPCE reverse current without damage shall be performed by test and analysis. The analysis shall be considered successful when the results show that no EPS is damaged by the abnormal reverse current flow as specified in the requirement [PQSV1015].

3.4.1.3.2 EPS FAULT PROTECTION

[PQSV1016V] Verification of overcurrent protection shall be verified by test and analysis. The test shall consist of loading the EPS source interface with resistive loads until the overcurrent protection clears the overcurrent condition. The verification shall be considered successful when the test shows the EPS source interface clears the overcurrent condition.

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight like configurations using appropriate circuit cables / connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits.

3.4.1.3.3 OVERVOLTAGE SURGE

[PQSV1017V] Verification of the overvoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the overvoltage surge at the EPS source side of the load interface remains within the limits specified in the requirement [PQSV1017] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the overvoltage at the EPS source interface is within the range specified in requirement [PQSV1017].

Rationale: This verification of the source surge is at the EPCE interface. Application and removal of a fault within the EPS can result in an overvoltage condition on other interface channels due to the line inductance between the source and the load.

3.4.1.3.4 UNDERVOLTAGE SURGE

[PQSV1018V] Verification of the undervoltage surge due to EPS fault shall be verified by test or analysis. The test or analysis shall be performed to verify the undervoltage surge at the EPS source side of the load interface remains within the limits specified in the requirement [PQSV1018] when subjected to the application and removal of a high current fault or other component failure. An analysis shall be performed to evaluate fault conditions where testing is not possible and could degrade flight hardware. The verification shall be considered successful when the test or analysis shows the undervoltage at the EPS source interface is within the range specified in requirement [PQSV1018].

Rationale: This verification of the source undervoltage is at the EPCE interface. Application and removal of a fault within the EPS can result in an undervoltage condition on other interface channels due to the line inductance between the source and the load.

3.4.1.3.5 EMERGENCY OPERATION

[PQSV1019V] Verification of EPS Emergency Operation shall be performed by analysis. The analysis shall verify that the EPS control and protection logic allows access to all available power sources during fault or component failure conditions.

3.4.1.3.6 FAULTS

3.4.1.3.6.1 HIGH IMPEDANCE FAULTS

[PQSV1020V] Verification of high impedance fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PQSV1020].

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight like configurations using appropriate circuit cables / connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits

3.4.1.3.6.2 HIGH CURRENT FAULTS

[PQSV1021V] Verification of high current fault protection shall be performed by test. The test shall consist of loading the EPS with a resistive load. The verification shall be considered successful when the test shows that the EPS clears the overcurrent condition within the time specified in the requirement [PQSV1021].

Rationale: Testing for the EPS switchgear will be performed on qualification hardware. Fault clearing capability for the switchgear will be performed in flight like configurations using appropriate circuit cables / connectors and resistive loads. Aggressive fault testing should not be performed on flight circuits

3.4.1.3.6.3 EPS, FAULT CONTAINMENT

[PQSV1022V] Verification of EPS fault containment shall be performed by analysis. The analysis shall consist of evaluating all branch circuits to verify that overcurrent protection is provided and trip coordination will prevent fault propagation and isolate faults. The verification shall be considered successful when the analysis shows that fault containment meets the requirement [PQSV1022].

3.4.2 ELECTRIC POWER CONSUMING EQUIPMENT INTERFACE

3.4.2.1 NORMAL OPERATION

3.4.2.1.1 STEADY STATE OPERATION

[PQSV2001V] Verification of EPCE operational compatibility with the steady-state voltage range shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PQSV2001]. EPCE shall be operated under selected loading conditions that envelop operational loading. The acceptable method to demonstrate compatibility with the minimum and maximum system voltage level is to test the EPCE at a steady-state input voltage of 98 Vdc (or below) and 136 Vdc (or above). The verification shall be considered successful when the test shows the EPCE operates nominally.

Rationale: EPCE undergoing susceptibility testing typically test at the low and high voltage with a voltage ripple superimposed.

3.4.2.1.2 EPCE POWER INTERFACE, NORMAL LOAD STEP TRANSIENT VOLTAGE

[PQSV2002V] Verification of compatibility with the normal load step transient at the EPS/EPCE interface shall be performed by test. Verification shall be performed by test at low and high input voltage values as specified in requirement [PQSV2002]. EPCE shall be operated under selected loading conditions that envelop operational loading. Rate of change should be between 0.5V/usec and 1V/usec. EPCE should be tested by applying an input voltage transient step as shown in the Normal Load Step-Down Transient Test and the Normal Load Step-Up Transient Test figures from the nominal steady-state voltage (120V) to the maximum transient levels (141V) and from a steady-state voltage of 114V to the minimum transient levels (93V). The Normal Load Step-Up Transient Test and Normal Load Step-Down Transient Test waveforms below depict the details. The verification shall be considered successful when the test shows the EPCE operates nominally when input terminals are subjected to test voltages as specified in Normal Load Step-Down Transient Test and Normal Load Step-Up Transient figures below.

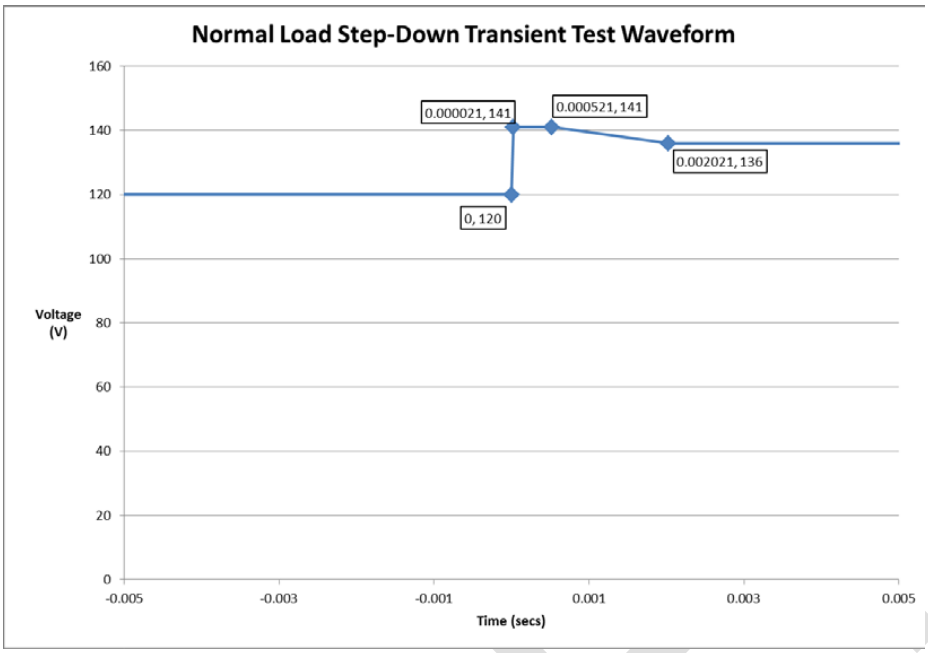


FIGURE 10 NORMAL LOAD STEP-DOWN TRANSIENT TEST

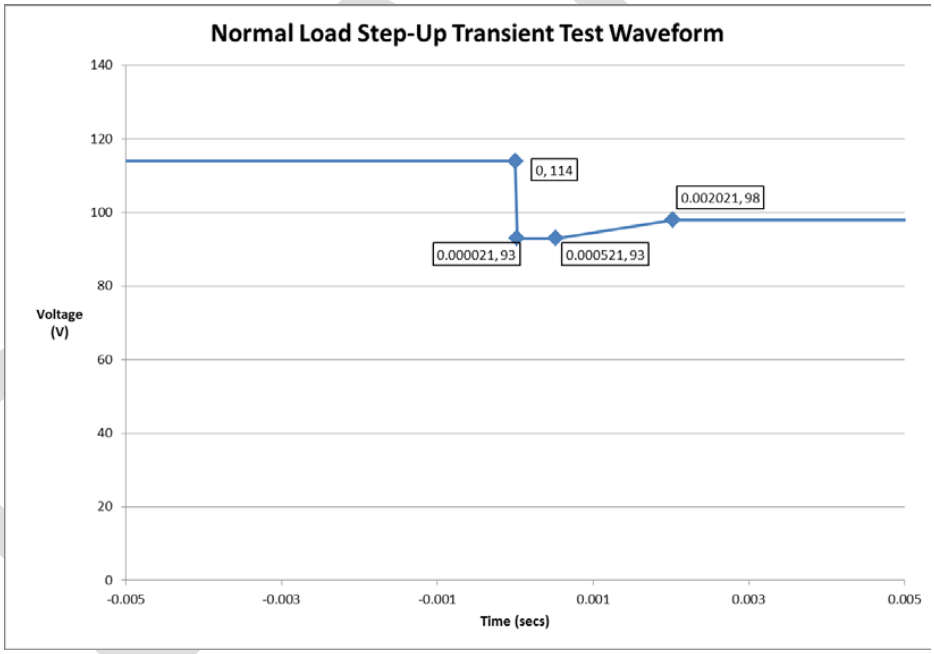


FIGURE 11 NORMAL LOAD STEP-UP TRANSIENT TEST

Rationale: The test conditions are at the loads interface.

3.4.2.1.3 EPCE, RIPPLE CURRENT

NVR

Rationale: Verification is considered successful by successfully performing the ripple tests as defined by the EMI control document.

3.4.2.1.3.1 EPCE, RIPPLE VOLTAGE SPECTRUM

NVR

Rationale: Verification is considered successful by successfully performing the spectrum tests as defined by the EMI control document.

3.4.2.1.4 STABILITY

NVR

3.4.2.1.4.1 LOCAL STABILITY

NVR

3.4.2.1.4.1.1 LARGE SIGNAL STABILITY

[PQSV2005V] Large signal stability shall be verified by test and analysis.

A large signal stability test shall be conducted for EPCE connected to the EPS source interface. An integrated analysis shall be provided for representative maximum and minimum load cases to demonstrate that impedance variations will not impact system stability. The input and transient response waveforms for the EPCE shall be recorded from the start of the pulse through the time when the transient diminishes to and remains below 10 percent of the maximum amplitude of the response. The input waveform shall be measured at the secondary side of the injection transformer.

The required test conditions may be produced using a programmable power source or the setup shown in Appendix E.4. Short-duration voltage pulses, as defined below shall be applied. Short-duration power-system transients are defined, as part of the Large Signal Stability requirement, as follows:

1) The rise and fall times (between 10 and 90 percent of the amplitude points) of the input voltage pulse shall be less than 1 microsecond.
2) Duration of the voltage pulse may vary between 20 microseconds and 125 microseconds in duration. In test, this shall be satisfied by applying pulses of duration of 20, 50, 80, 100, and 125 microseconds (±5 microseconds).
3) Magnitude of the voltage pulses imposed on top of 120.0 ± 1.0 Vdc input shall be 14.5 ± 0.5 volts, positive. Subsequently, the resulting transient amplitude will remain within the EPS normal load step transient limits.

The defined transient is illustrated in the Large Signal Stability Test Transient figure and appears in series with the output of the power source as shown in Appendix E.4.

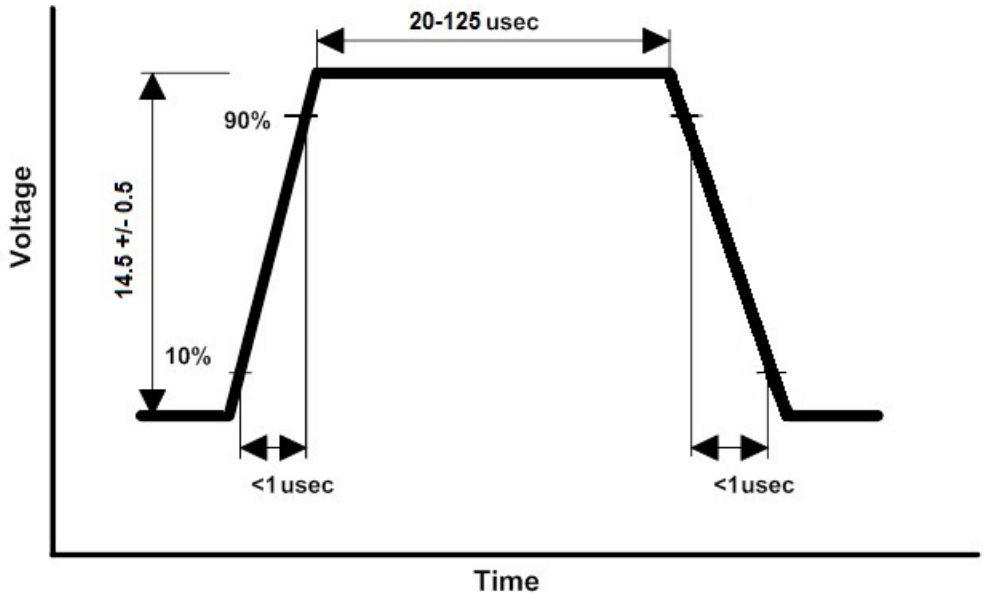


FIGURE 12 LARGE SIGNAL STABILITY TEST TRANSIENT

The verification shall be considered successful when results show that transient responses, measured at the input to EPCE, diminish to 10 percent of the maximum amplitude within 1.0 milliseconds and remain below 10 percent thereafter as illustrated in the Large Signal Stability Transient Response figure. The connected EPCE shall maintain full performance as specified during the resulting transients.

For the analysis method of verification, the analysis model must be a high fidelity time domain model (which includes the voltage and/or current control loops of the converter) in order to properly capture the voltage transient response when subjected to the large signal stability pulse.

3.4.2.1.4.1.2 EPCE INPUT IMPEDANCE

[PQSV2006V] Verification of EPCE input impedance shall be performed by test. See Appendix E.1. EPCE impedance shall be verified by measuring the normalized input impedance magnitude and phase at low and high input voltage values as specified in the requirement [PQSV2006].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE.

3.4.2.1.4.1.3 SMALL SIGNAL STABILITY

[PQSV2007V] Verification of EPCE Small Signal Stability at the EPS source interface shall be performed by test and analysis. EPCE Small Signal Stability shall be verified by calculating the complex impedance ratio of the source impedance divided by the load impedance and ensuring that it remains outside the hatched area (Forbidden Zone) shown in Nyquist Stability Plot of ZS divided by ZL, from 30 Hz to 100 kHz. EPCE shall be operated under selected loading conditions that envelop operational loading. The verification shall be considered successful when the analysis supported by test data

shows the ZS divided by ZL ratio for all defined EPCE interfaces do not cross into the Forbidden Zone defined in requirement [PQSV2007].

Rationale: This requirement needs to be met with all reasonable combinations of ON/OFF states and operating modes of the electrical loads within the same EPCE. A basis calculation example, test setup for Input Impedance tests to measure both magnitude and phase curves, are described in Appendix E.

3.4.2.1.5 STARTUP AND INRUSH

3.4.2.1.5.1 CURRENT LIMITING SWITCHGEAR COMPATIBILITY

[PQSV2008V] Verification of the current limiting source compatibility shall be by test. The test shall consist of the DUT operating with current limiting source switchgear that limits current to 110% of the test current as the test source. The DUT shall not exhibit any malfunction, degradation of performance, or deviation from specified parameters when operated per requirement [PQSV2008].

3.4.2.1.5.2 INRUSH/SURGE CURRENT TRANSIENTS

[PQSV2009V] Verification of allowable EPCE inrush and surge transient shall be performed by test and analysis using a characteristic non-current limiting source and a source that limits current to 110% of the test current as the test source. The test or analysis shall be performed as illustrated in Appendix E.2 to verify that the DUT inrush current during initial voltage application and surge current during DUT operation remains within the magnitude and duration limits specified in requirement [PQSV2009] when using the non-current limiting and current limiting (110%) source. The verification shall be considered successful when the results show that the transient remains within the limits specified in the requirement [PQSV2009].

3.4.2.1.6 REVERSE CURRENT

[PQSV2010V] Verification of EPCE reverse current shall be performed by test and analysis. The test or analysis shall be performed on EPCE circuitry to show that during normal operation there are no reverse currents that will flow from the EPCE back into the EPS. The test and analysis shall be performed as illustrated in Appendix E.2. The analysis shall be considered successful when the results show that no EPCE reverse current flows as specified in the requirement [PQSV2010].

3.4.2.1.7 EPCE INPUT ISOLATION

[PQSV2011V] Verification of power source isolation shall be performed by test and analysis. EPCE equipment shall be tested to the specified limits for dielectric isolation between power sources and between power sources and chassis. Analysis of the design shall be performed to determine no single failure can cause loss of isolation.

3.4.2.2 ABNORMAL OPERATION

3.4.2.2.1 ABNORMAL REVERSE CURRENTS

[PQSV2012V] Verification of EPCE reverse current shall be performed by test and analysis. The test and analysis shall be performed as illustrated in Appendix E.2 on EPCE circuitry to determine the amount of current that will flow from the EPCE back into EPS during a simulated system voltage droop and EPS fault condition. The test or analysis shall be considered successful when the results show that EPCE limits reverse current flow as specified in the requirement [PQSV2012].

3.4.2.2.2 OVERVOLTAGE SURGE

[PQSV2013V] Verification of compatibility with the overvoltage surge at the EPS loads interface shall be performed by test and analysis. The test or analysis shall be performed with the EPCE subjected to an input transient as specified in requirement [PQSV2013]. EPCE should be tested from the maximum steady-state voltage (136V) to the maximum transient levels (150V) and back to the maximum steady-state voltage (136V). The Overvoltage Transient Test Waveform depicts the voltage and time steps. The verification shall be considered successful when the test or analysis shows the EPCE operates nominally per the EPCE controlling documents after subjected to the overvoltage surge as specified in requirement [PQSV2013].

Rationale: This verification of the source surge is at the EPCE interface.

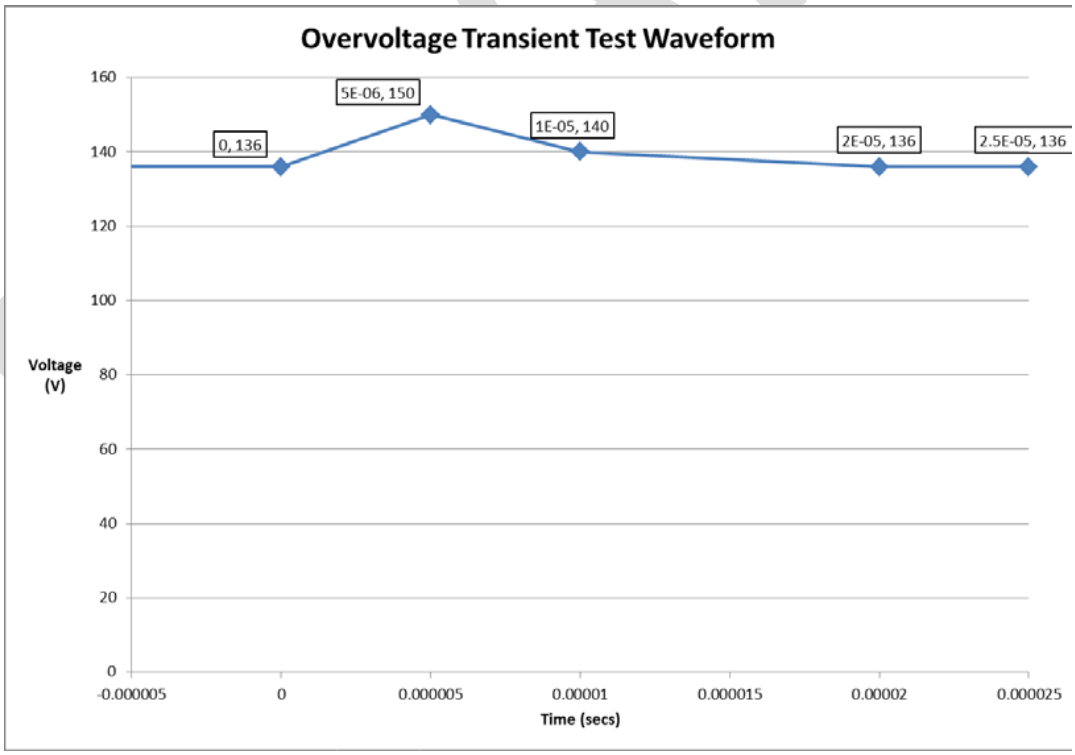


FIGURE 13 OVERVOLTAGE TRANSIENT TEST WAVEFORM

3.4.2.2.3 UNDERVOLTAGE SURGE

[PQSV2014V] Verification of compatibility with the undervoltage surge at the EPS loads interface shall be performed by test and analysis. The test or analysis shall be performed with the EPCE subjected to an input transient as specified in requirement [PQSV2014]. EPCE should be tested from the steady-state voltage (120V) to 0V and back to the steady-state voltage (120V). The Undervoltage Transient Test Waveform depicts the voltage and time steps. Rate of change should be between 0.5V/microsecond and 1V/microsecond. The verification shall be considered successful when the test or analysis shows the EPCE operates nominally per the EPCE controlling documents after being subjected to the undervoltage surge as specified in requirement [PQSV2014].

Rationale: This verification of the source undervoltage is at the EPCE interface.

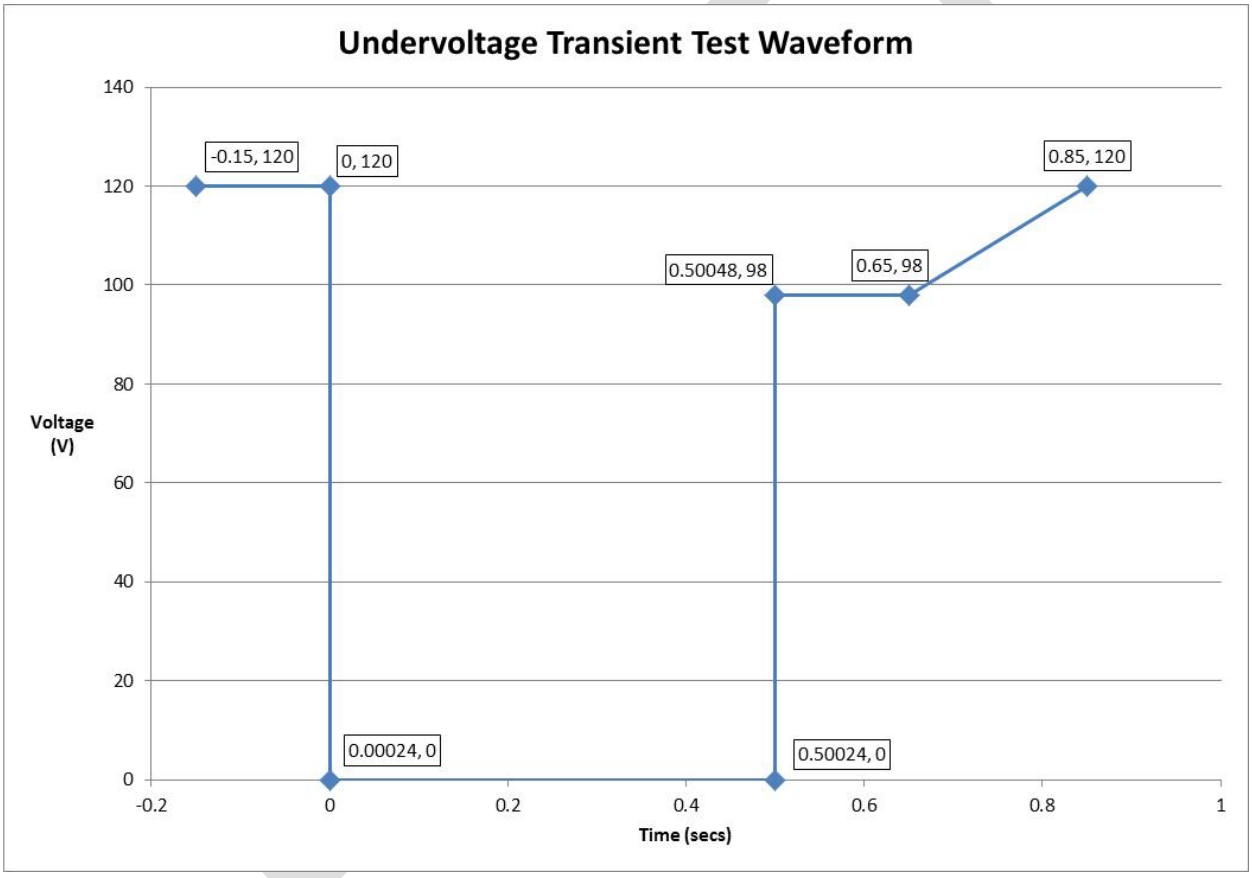


FIGURE 14 UNDERVOLTAGE TRANSIENT TEST WAVEFORM

3.4.2.2.4 EMERGENCY OPERATION

[PQSV2015V] Where specified, EPCE operation with an emergency voltage input of 95 V shall be verified by test.

4.0 FUTURE TOPICS FOR POSSIBLE STANDARDIZATION

N/A

APPENDIX A ACRONYMS AND ABBREVIATIONS

AC	alternating current
A	Ampere
dB	decibels
DC	direct current
DUT	device under test
E3	Electromagnetic Environmental Effects
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interface
EPCE	Electrical Power Consuming Equipment
EPS	Electrical Power System
EUT	Equipment Under Test
FET	Field Effect Transistor
GSE	Ground Support Equipment
Hz	Hertz
kHz	kilohertz
MCB	Multilateral Coordination Board
MHz	Megahertz
µs	microsecond
NVR	No Verification Required
POR	Point of Regulation or Point of Reference for unregulated systems
pps	pulses per second
PU	Per Unit
RC	Resistor/Capacitor
rms	root mean square
TBD	To Be Determined
TBR	To Be Resolved
µF	microfarad
V DC	Volt direct current
V p-p	Volts peak-to-peak
W	Watt
Zn	normalized input load impedance

APPENDIX B GLOSSARY

ABNORMAL OPERATION

Abnormal operation is that condition of the EPS wherein a fault or failure in the EPS distribution wiring, or connected loads, has occurred and the protective devices of the EPS are operating to isolate or remove the fault from the appropriate EPS interface.

BRANCH CIRCUIT

A power distribution line that delivers power from an overcurrent protection device to an electrical load device.

BUS CONTROL

A means of controlling the direction and flow of current across an interface.

CLEARING TIME

The time for an overcurrent protection device to interrupt a circuit fault.

CURRENT LIMITING

The process of actively controlling the flow of electrical current to a level at, or below, a defined threshold when it might otherwise be exceeded. Also, the role of electrical protection controls that perform this function.

DISTRIBUTION SYSTEM

The means to distribute power through the power system.

DROP-OUT TIME

Drop-out time is the time interval during which the electric power is interrupted. Voltages will be below defined values for the duration of the drop-out and are assumed to fall to zero Volts.

ELECTRIC POWER CONSUMING EQUIPMENT

EPCE is used in this document as a generic term to refer to any piece of electrical equipment acting as a load on the Spacecraft.

ELECTRIC POWER SYSTEM

The EPS consists of the electric power generation and distribution subsystems, including all devices up to the EPCE power interface such as generators, energy storage devices, cables, switches, protective devices, converters, and regulators.

ELECTROMAGNETIC COMPATIBILITY

The ability of systems, and EPCEs that are exposed to or use the electromagnetic spectrum to operate in the operational environments without suffering unacceptable degradation or causing unintentional degradation because of electromagnetic radiation.

EMERGENCY OPERATION

Emergency operation occurs upon failure of a primary power generation/energy storage system and/or contingency cases requiring deep discharges users of electrical power.

EPS POWER INTERFACE

The EPS Power Interface is the point of connection for a fixed EPCE. For portable equipment, the EPS power interface is at the EPS receptacle.

FAULT

A condition causing overcurrent on the EPS.

FAULT CLEARING

The action in power system protection devices that disconnects a faulted line from the rest of the system.

FAULT CONTAINMENT

A mechanism to localize a circuit fault to the closest protective device.

FAULT COORDINATION

Coordinating a series of protective devices in such a way as to make sure the protective device nearest to the fault clears the fault before affecting upstream switchgear.

FEEDER LINE

Cables that distribute electrical power from a primary bus to lower level protective switchgear.

GROUND

Common circuit reference point considered to have 0 V.

HIGH CURRENT FAULT

A fault condition that produced very high currents generally conducting fault current through a hard physical connection. This condition is often referred to as a "bolted fault."

HIGH IMPEDANCE FAULT

A fault condition that produces unacceptable currents but is not considered high currents. This fault is often considered the most dangerous and difficult to clear. This fault is often referred to as a "soft fault."

IMPEDANCE

Electrical impedance describes the amplitudes of the voltage, current, and phase. Impedance is the complex quantity $\dot{Z}$.

INRUSH CURRENT

Inrush current is defined as EPCE initialization current to energize loads or portions thereof. The current envelope is the total charging current in amp-seconds that starts at the instant current exceeds the rated load current of the EPCE and ends once the input current returns to the rated load current value.

INSTABILITY

Characterized by an output or internal state of a system growing without bounds.

INTERFACE POWER

The electrical power supplied/consumed to/from an electrical load.

LEAKAGE CURRENT

Current flow as a result of imperfect insulation or semiconductor materials.

LOCAL STABILITY

A limited measure of EPCE stability under representative (or typical) source impedance conditions.

NOMINAL RATING

An approximate value used to indicate its intended application or to differentiate it from similar devices with different ratings.

NUISANCE TRIPPING

An inadvertent interruption of an EPCE by the protection switchgear during normal operation of the load.

NORMALIZED INPUT IMPEDANCE

EPCE Input impedance curve scaled to 0 dB (1 ohm) at zero frequency.

OVERCURRENT

A situation where larger than intended electric currents exist in a circuit.

OVERCURRENT PROTECTION

The limiting of excessive circuit current by some means.

OVERVOLTAGE

A potentially hazardous condition when the voltage in a circuit or part of it is raised above the system upper design limit.

PEAK RIPPLE VOLTAGE

The absolute value of the maximum difference between the steady state and instantaneous voltage. The peak ripple voltage is the sum total peak voltage amplitude of a ripple composite, including non-periodic events that can be present on the EPS for a fixed bandwidth.

PEAK-TO-PEAK VOLTAGE

A voltage measurement of a periodic voltage waveform from the lowest well to the highest point (peak).

POWER QUALITY

Electrical characteristics that allow the system to function properly without significant loss of performance or life.

PULSED LOADS

EPCE that operates in a periodic manner with a frequency below 30 Hz.

RATED LOAD CURRENT

The maximum current draw from a load after all start-up or mode change transients have settled out.

RATED POWER

The nominal output power for EPS branch circuits or power consumption of an EPCE.

REPRESENTATIVE LOAD

EPCE that can be either constant power or resistive that stresses the power source to verify performance envelope compliance.

REVERSE CURRENT

Direct current flowing in the opposite direction from the intended circuit design. For loads, this can be created from the energy discharge of a circuit due to counter electromagnetic force due to regenerative loads (such as motor controllers or actuators) or under a fault condition upstream of the load power interface.

RIPPLE VOLTAGE AMPLITUDE

Ripple voltage is the RMS value of all ac voltage components that are superimposed on the steady-state dc voltage.

RIPPLE VOLTAGE SPECTRUM

The frequency distribution of ripple voltage components.

SHORT CIRCUIT

Abnormal low impedance/resistance connection between nodes of an electrical circuit at different voltages.

SINGLE-POINT GROUND

Single-Point Ground is a single ground reference to structure.

STABILITY

The quality of electrical device operation wherein key characteristics resist deviation from intended values under both static and dynamic conditions.

SURGE CURRENT

Surge current is defined as a transient, or pulsed, current, due to operation of an EPCE that is greater than the average over any interval of time.

SWITCHGEAR

The combination of electrical/electronic disconnects or fuses used to operate/isolate electrical equipment. Switchgear can be designed to both operate and protect (clear circuit faults) equipment.

TRANSIENT RESPONSE

A disturbance in an electrical system brought about by a sudden change of load.

TWO-WIRE

An electrical distribution system using separate supply and return conductors to supply electrical power to an EPCE.

VOLTAGE DROOP

The reduction in output voltage due to a fault or failure.

VOLTAGE SPECTRUM

A graph of individual voltage intensity components plotted against frequency.

APPENDIX C - OPEN WORK

Table C-1 lists the specific To Be Determined (TBD) items in the document that are not yet known. The TBD is inserted as a placeholder wherever the required data is needed and is formatted in bold type within brackets. The TBD item is numbered based on the section where the first occurrence of the item is located as the first digit and a consecutive number as the second digit (i.e., <TBD 4-1> is the first undetermined item assigned in Section 4 of the document). As each TBD is solved, the updated text is inserted in each place that the TBD appears in the document and the item is removed from this table. As new TBD items are assigned, they will be added to this list in accordance with the above described numbering scheme. Original TBDs will not be renumbered.

TABLE C-1 TO BE DETERMINED ITEMS

TBD	Section	Description

Table C-2 lists the specific To Be Resolved (TBR) issues in the document that are not yet known. The TBR is inserted as a placeholder wherever the required data is needed and is formatted in bold type within brackets. The TBR issue is numbered based on the section where the first occurrence of the issue is located as the first digit and a consecutive number as the second digit (i.e., <TBR 4-1> is the first unresolved issue assigned in Section 4 of the document). As each TBR is resolved, the updated text is inserted in each place that the TBR appears in the document and the issue is removed from this table. As new TBR issues are assigned, they will be added to this list in accordance with the above described numbering scheme. Original TBRs will not be renumbered.

TABLE C-2 TO BE RESOLVED ISSUES

TBR	Section	Description

APPENDIX D – SYMBOLS DEFINITION

N/A

APPENDIX E – TEST METHODS

E.1 INPUT IMPEDANCE MEASUREMENTS

EPS source interface is the point where user loads will be connected to the power system. The test described in this section is the suggested test setup to measure load impedance at the EPS source interface. It is important to understand that the load impedance measurement test setup will include a simulated source and the EPCE under test. The EPCE input impedance can be measured by injecting an AC signal to the system using either of two methods: series voltage injection and parallel current injection.

Generally, the load input impedance is greater than the source output impedance in magnitude. The Test Setup for Impedance Measurement Using Series Voltage Injection figure shows a typical test setup for series voltage injection method. This method works better for measuring load input impedance because most of the injected voltage signal is applied to the high impedance in the load side. The figure shows the measurement of load impedance at the input terminals of an EPCE. Note: it is recommended to place the load on a non-conductive surface when performing this test to avoid effects caused by any common mode capacitance within the load.

Analysis Steps:

1) Determine the Base DC Input Impedance, Z_{rated}, of the EPCE at the worst case operating condition. This condition will normally be operation at minimum input voltage and maximum load of the EPCE. Vrated is the rated voltage of the EPCE and I_{rated} is the rated steady-state EPCE current.

   i) $Z_{rated} = V_{rated} / I_{rated} = (V_{rated})^2 / P_{rated}$

2) Obtain Bode Plots for the Magnitude and Phase of the impedance versus frequency for each test condition.

3) Determine per unit Magnitude, $Z_{perunit}$, by dividing the magnitude values of each plot by the value of Z_{rated} obtained in step 1. The resulting plots will represent the magnitudes in per unit ohms after converting to dB ohms.

   ii) $Z_{perunit} = Z_{actual} / Z_{rated}$

   iii) $Z_{perunit}$ dB Ohms = 20 X log ($Z_{perunit}$)

NOTE: Note that other equivalent test support equipment can be used for the Impedance test.

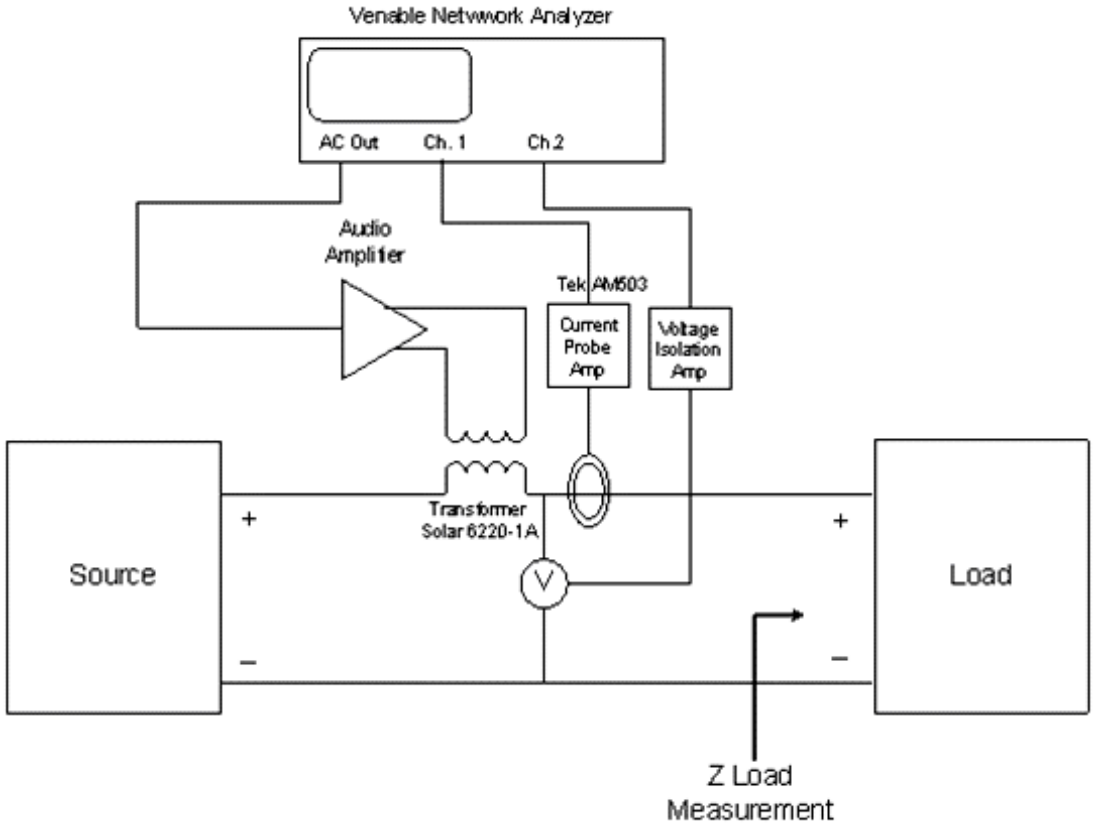


FIGURE 15 TEST SETUP FOR IMPEDANCE MEASURE USING SERIES VOLTAGE INJECTION

Example 1: Example Input Impedance Magnitude of Load figure shows the input impedance magnitude of a load which is rated at 177 W. The base impedance, Zrated = 98^2 / 177 = 54.26 ohms. The per-unit impedance (Example $Z_{perunit}$ Input Impedance Magnitude of Load) on this load is obtained by dividing the actual impedance magnitude, Z_{actual}, (Example Input Impedance Magnitude of Load figure) by Z_{rated} and converting the results into dB (dB Ohms = 20*log($Z_{perunit}$)). Example $Z_{perunit}$ Input Impedance Magnitude of Load figure also compares the per-unit input impedance of this load to the requirement.

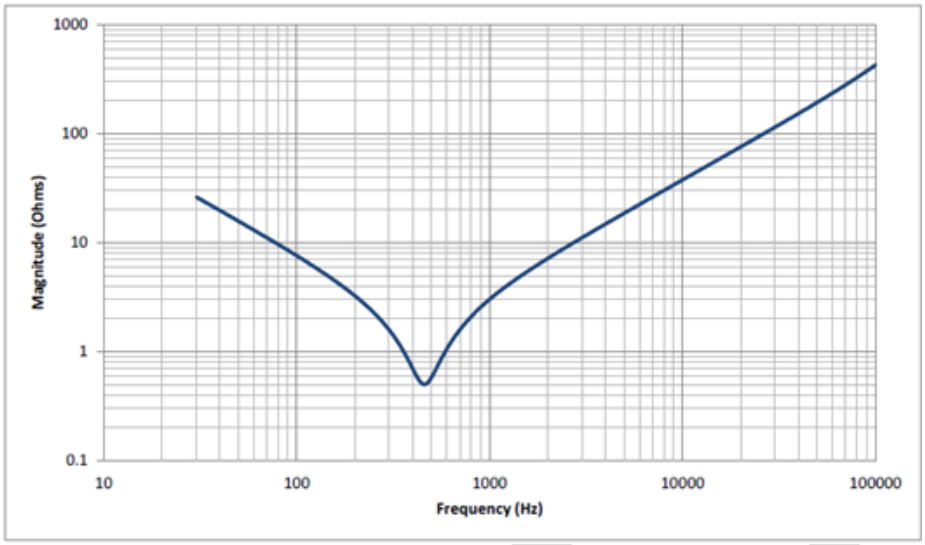


FIGURE 16 EXAMPLE INPUT IMPEDANCE MAGNITUDE OF LOAD

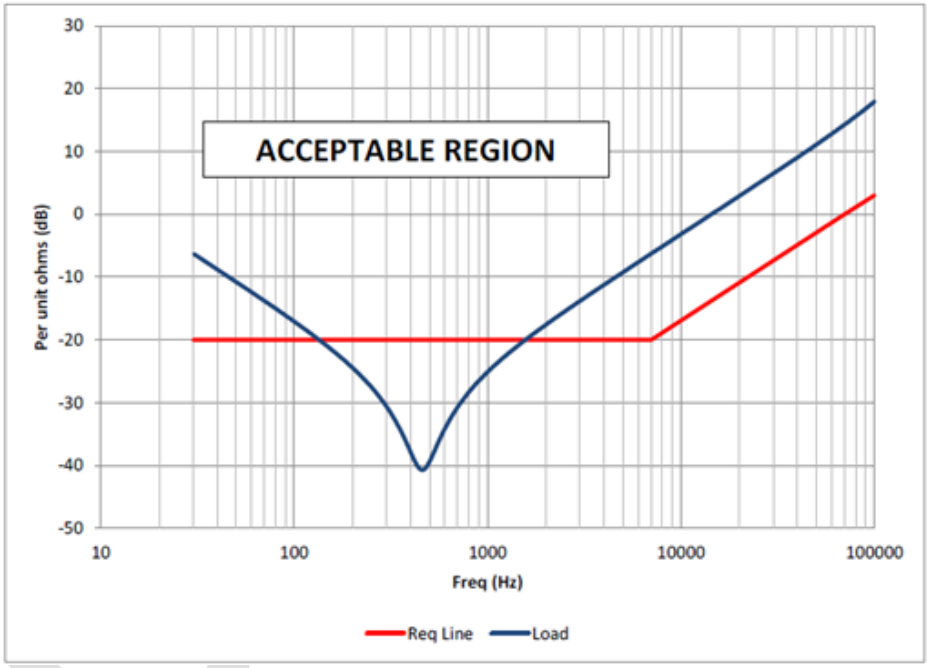


FIGURE 17 EXAMPLE $Z_{PERUNIT}$ INPUT IMPEDANCE MAGNITUDE OF LOAD

E.2 LOAD STEADY-STATE , INRUSH, SURGE AND REVERSE CURRENT

Figure 18 shows a typical test setup for measuring voltage and current at the EPCE input terminals. Other test support equipment can be used. The power supply output ratings must be high enough that the measured surge currents are not limited by its output capacity for the load and inrush test. The power supply for reverse current must be output current limiting with adequate capacity to supply steady state load current.

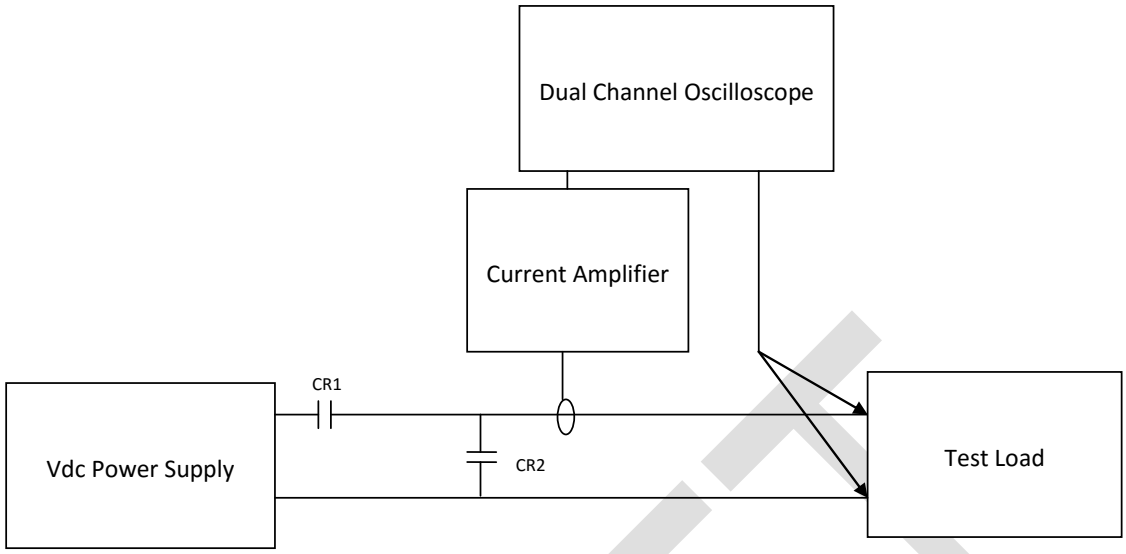


FIGURE 18 TYPICAL TEST SETUP FOR INRUSH, SURGE, AND REVERSE CURRENT MEASUREMENTS

NOTE: A stiff power source is required for this test. Capacitance may be added to stabilize the source.

The voltage sag, δV due to transient inrush current at the input to the DUT should meet the following inequality:

$$\delta V \le (V_{nominal} - V_{minimum}) \bullet \sqrt{\left(\frac{I_{SS}}{I_{bus}}\right)}$$

Where,

$V_{nominal}$ = nominal bus voltage

$V_{minimum}$ = specified minimum bus voltage

I_{SS} = DUT steady-state current draw

I_{bus} = power bus maximum steady state draw

E.2.1 TYPICAL RATED LOAD, INRUSH, OPERATION WITH CURRENT LIMITING SWITCHGEAR AND NORMAL REVERSE CURRENT TESTING PROCEDURES

E.2.1.1 RATED LOAD AND INRUSH CURRENT

Current limiting devices will not be present in the line between the power supply and the EPCE under test.

a) With relay CR1 open, energize the power supply.

b) With the DUT configured to draw maximum power, close the CR1 relay to energize the DUT, record the inrush current and voltage.

c) Allow sufficient time for a steady state condition, record the load current.

d) De-energize the power supply, record the normal reverse current.

e) Measure and record the current and voltage waveforms.

E.2.1.2 OPERATION WITH CURRENT LIMITING SWITCHGEAR

a) Replace CR1 with a relevant current limiting device ($CR1_{CL}$) in the line between the power supply and the EPCE under test.

b) With $CR1_{CL}$ open, energize the power supply.

c) With the DUT configured to draw maximum power, close the $CR1_{CL}$ to energize the DUT, record the inrush current.

d) Allow sufficient time for a steady state condition, record the rated load current.

e) De-energize the power supply, record the normal reverse current.

f) Measure and record the current and voltage waveforms.

E.2.1.3 REVERSE CURRENT DURING A CIRCUIT FAULT

It is recommended that CR1 and CR2 be solid state switches with the capability to source and sink the required currents.

a) With relay CR1 open, energize the power supply.

b) With the DUT configured to draw maximum power, close the CR1 relay to energize the DUT and allow the DUT to reach steady state operation.

c) Open CR1 and Close CR2 – This transition must be within 5 µs.

d) Measure and record the current and voltage waveforms.

E.2.2 ANALYSIS

The inrush and reverse current waveform may be digitized to allow computation of the ampere-seconds value by numerical integration. The resulting input current and voltage waveforms, to the EPCE, can be used to validate computer models used in analysis.

E.3 SOURCE IMPEDANCE MEASUREMENT

The tests described in this section are suggested test setups to measure EPS source impedance. A single test at nominal load may be adequate for passive sources such as a battery or fuel cell. Active sources such as DC/DC converters, usually require tests over a range of load currents (<10% load to full load).

Figure 19 illustrates two source impedance test methods. A network analyzer is connected to measure the AC components of the source voltage and output current. The analyzer output provides a signal to modulate the load current. Either square wave or sine wave modulation may be used, depending on the network analyzer used.

If the audio amplifier and transformer shown in Figure 19(a) are available, the Parallel Current Injection method may be used. The amplifier output modulates the load current and the voltage and current sensors provide input to the analyzer.

The setup in Figure 19(b) uses a resistor-transistor combination to provide load current modulation. For sine modulation, the analyzer output drives the gate of power FET Q1 with R1 connected to the source terminal to form a modulated current sink. Optional

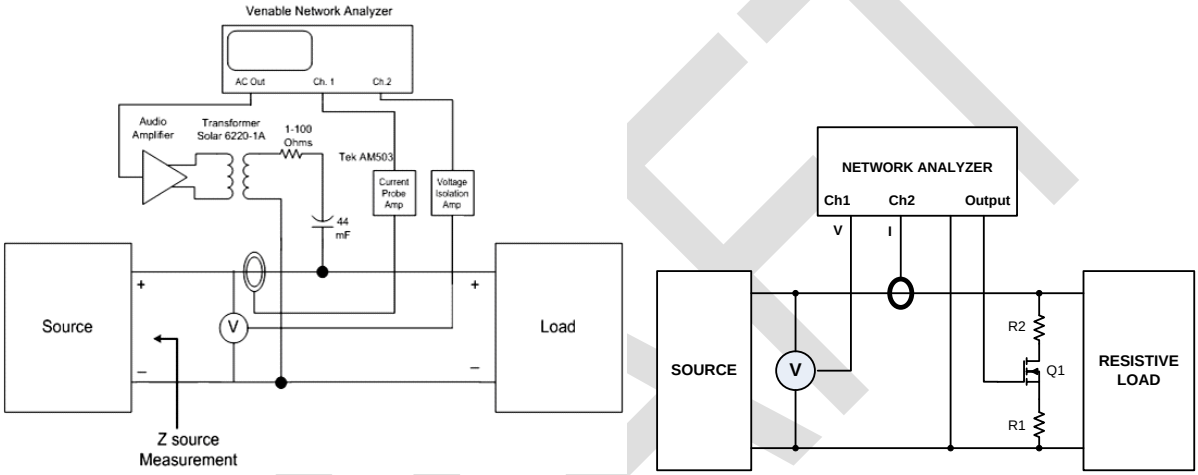
resistor R2 reduces the voltage and the power dissipation in Q1. For square wave modulation, R1 = 0 and Q1 acts as a switch with low power dissipation. R2 Is selected to provide the desired level of load modulation.

Test Steps:

Configure the network analyzer to calculate $Z_{source} = V_{ac}/I_{ac}$, where V_{ac} and I_{ac} are the AC components of the measured voltage and current.

Set the resistive load to the desired value.

Obtain Bode plots for the magnitude and phase of the impedance versus frequency for each load condition.



(a) Parallel Current Injection (b) Constant Current or Resistive Load Injection

FIGURE 19 SOURCE IMPEDANCE MEASUREMENT TEST SETUPS

E.4 LARGE SIGNAL STABILITY

A typical large signal stability test setup is the Large Signal Stability Test Setup figure. The pulse generator/amplifier, with source impedance of less than 0.2 ohms from 100 Hz to 10 kHz, must provide power to the 2-ohm load of the primary side of the pulse transformer. Short-duration power-system transients per [PQSV2005V] should be applied. An alternate test set-up can be the same as used for the normal and abnormal voltage transient tests.

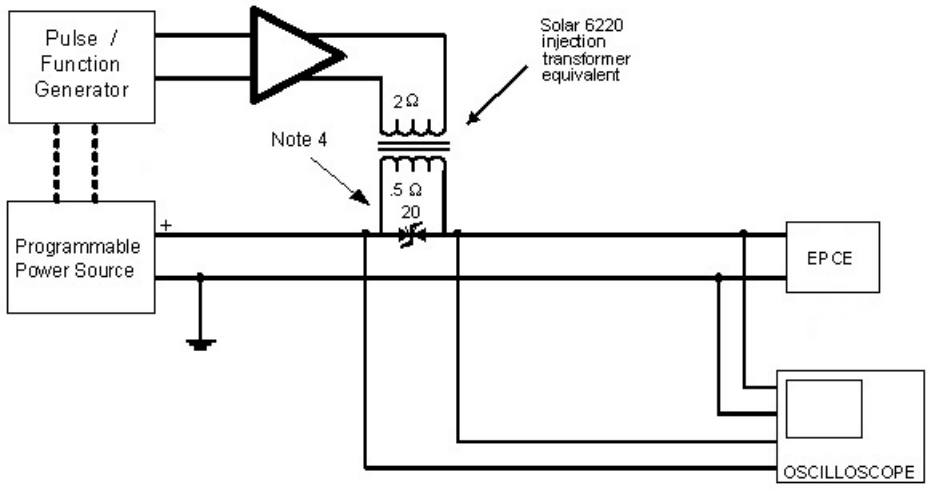


FIGURE 20 LARGE SIGNAL STABILITY TEST SETUP

NOTE:

1. The output of the pulse generator must be applied to the transformer through a drive amplifier that has less than 0.2-ohm output (source) impedance from 100 Hz to 10 kHz.
2. The drive amplifier should be capable of delivering at least 75 watts into a 4-ohm load.
3. A differential probe is used if the scope is grounded.
4. Pulse generator, injection transformer and Zener diode may require adjustment to generate the test pulses and to protect the EPCE under test.
5. The power source should be representative of the power environment.

APPENDIX F – GENERAL DISCUSSION

F.1 POWER QUALITY

Power quality, as defined, includes ripple voltage, time transient system response, and bus voltage operation range. Nominal dc voltage is generally not considered power quality but more of a system definition. The time varying nature of power quality affects this nominal voltage to create the "Steady-state Normal" voltage range used within this standard. EPCE designers must address the ripple voltage effects and contributions from the attached loads, load modulations, and radiated susceptibility. Switching of power sources, distribution switchgear, converters, and regulators provide a base "source" ripple voltage that is inherent with the power system. The next source of ripple is reflective ripple from the loads themselves back onto the power system. Load modulation ripple due to loads that are modulated or pulsed, repeatedly switched off to on, whether by nature or due to external effects, when large enough, can cause voltage overshoot and undershoot when operating. An example of modulated loads can be the docking mechanisms used for vehicle docking. Finally, ripple voltage due to radiated susceptibility can be impressed on the power system from a radiated source where the influences are dependent on the geometry of the power system.

To minimize unnecessary designer constraints, the system frequency spectrum was adopted as a worst-case design benchmark for ripple voltage.

F.2 PORTABLE LOADS

Special considerations are needed by the electric power consumer user when using an extension cord and multi-outlet power strips. The power quality at this interface can be adversely affected by misapplication of this requirement. Loads with high inrush current, high peak power to average power ratio, and high current ripple amplitude can adversely affect the power quality at this interface by degrading electric power characteristics. Power quality problems are exacerbated when multiple portable loads are connected to a single multi-outlet power strip, with loads not coordinated, causing voltage sag, current limiting, and voltage dropout, essentially a loss of power quality. The total aggregate electrical loading when using a multi-outlet power strip should be taken into consideration with respect to the upstream power feed. Voltage droop, voltage dropout, and the normal/abnormal system transients can be associated with this interface when loads are misapplied. The EPCEs connected to this interface need to be designed to operate through or not suffer damage or cause an unsafe condition due to this abnormal power quality.

F.3 CAPACITIVE LOADS

Large capacitive input filters or loads can have a stabilizing effect on the EPS, although excessive capacitance can create voltage droop during power-up. Loads with large input capacitance must be coordinated with protective switchgear. The user must ensure that these capacitance limits are not exceeded on a per channel basis.

F.4 INDUCTIVE LOADS

Large inductive loads, such as large solenoids, stepper motors, valves, contactors, etc., require voltage transient suppression to control EMC emissions and reverse energy requirements. Large inductive loads when combined with constant power converters can cause output tripping when the current demand is not coordinated with the protective switchgear.

F.5 STABILITY CRITERIA – SMALL SIGNAL STABILITY APPROACH

A typical cause of system instability is negative impedance load. This negative impedance occurs in systems that frequently include constant power loads. As long as a negative impedance load is powered by an ideal voltage source (with very low output impedance), the system is stable. However, in cases in which the load is powered by a non-ideal source whose output impedance amplitude is larger than the negative load impedance, the whole system may become unstable.

For checking small-signal system stability, the concept of an impedance criterion was adopted by the designers of filter-switching regulators with input filters. The concept was found to be useful in analyzing the stability of distributed power systems at the interface between the source subsystem and the load subsystem. At the system level, impedance specifications for each subsystem can be defined based on the requirements for system stability. At the component level, knowledge of the Input/Output (I/O) impedance characteristics of a module/subsystem is required to meet the specifications for system stability.

Figure 21 shows a system with source and load Impedances. Z_S is the output impedance of the source subsystem, Z_L is the input impedance of the load subsystem.

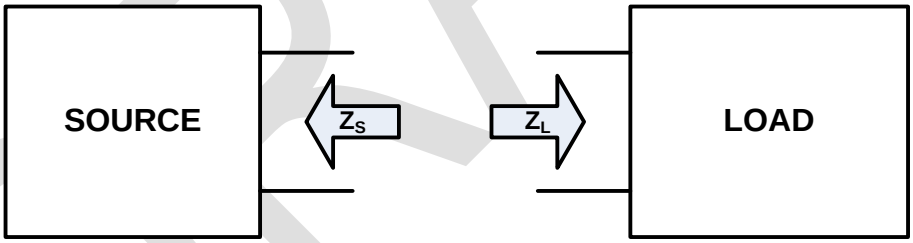


FIGURE 21 SERIES INTEGRATION OF TWO SUBSYSTEMS

When the source is connected to the load, the parallel combination of Z_S and Z_L is given by:

$$Z = \frac{Z_S \cdot Z_L}{Z_S + Z_L} = \frac{Z_S}{\frac{Z_S}{Z_L} + 1}$$

If $|Z_S| < |Z_L|$ for all frequencies, then the system is stable. When $|Z_S| > |Z_L|$, further analysis is needed to determine system stability. The Nyquist criterion can then be applied to determine a less conservative criterion that assures system stability.

According to the Nyquist criterion, small-signal system stability can be determined by whether the curve of Z_S/Z_L circles the (-1,0) in the S-plane as shown in Figure 22.

A forbidden region on this diagram establishes a system stability margin.

By keeping Z_S/Z_L out of the forbidden region as shown in the figure, small signal stability can be assured.

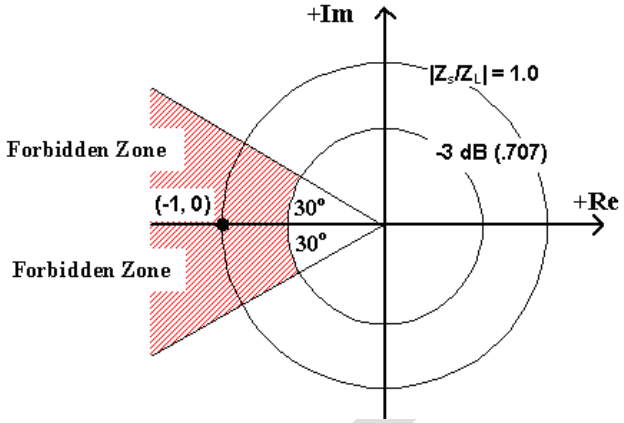


FIGURE 22 FORBIDDEN ZONE FOR Z_S/Z_L